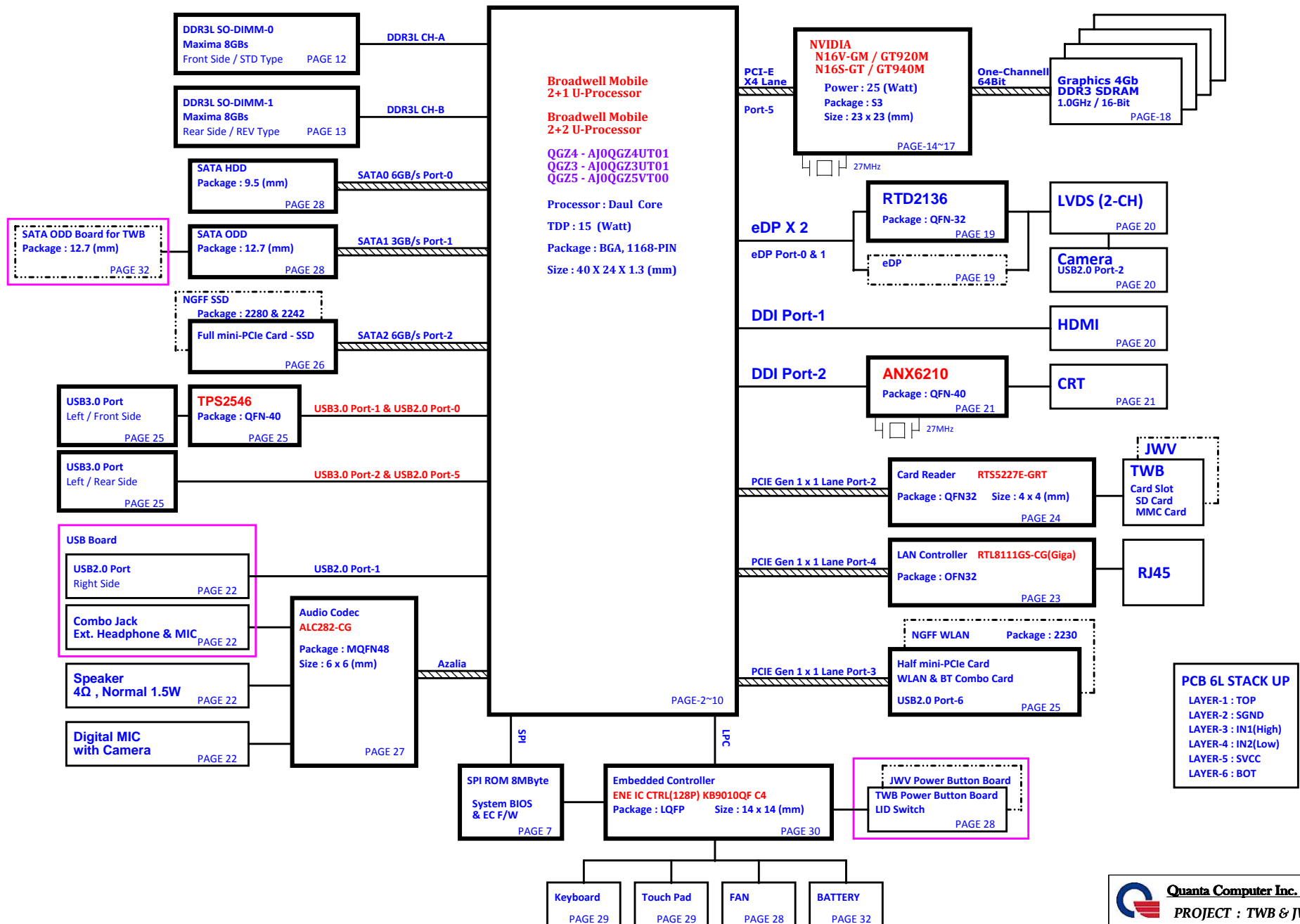
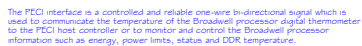


TWB + JWV Intel Boardwell ULT Platform Block Diagram





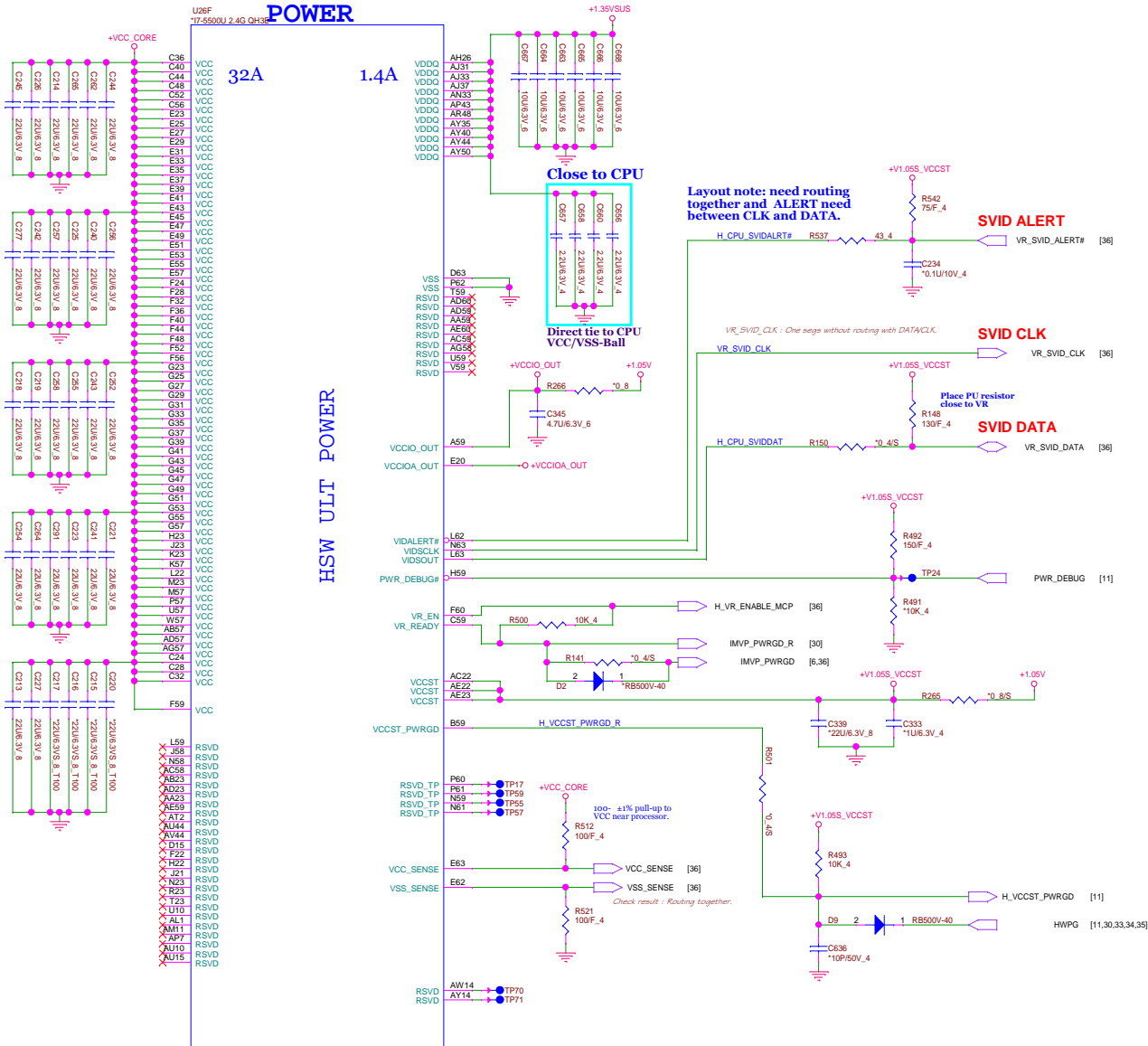
POWER

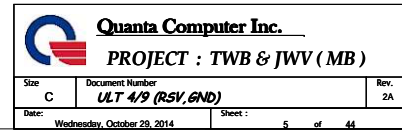
U08F
17-5500U 2.4G QHSE

32A

1.4A

HSW ULT POWER

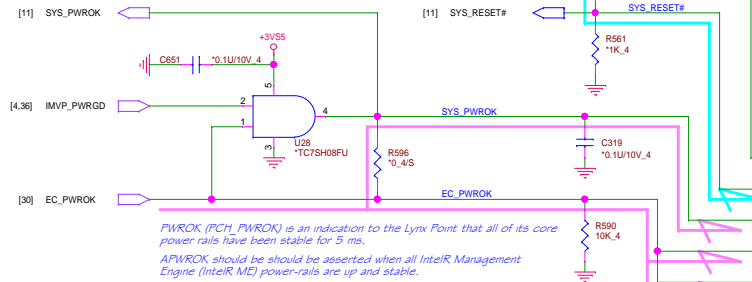




Lynx Point-LP Platform Controller Hub (LVDS,DDI)

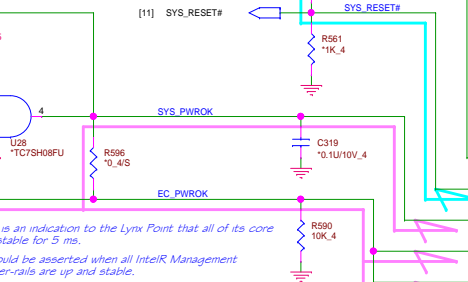
System PWR_OK(CLG)

SYS_PWROK is used to inform the Lynx Point that power is stable to some other system component(s) and the system is ready to start the exit from reset.



SYS_RESET#

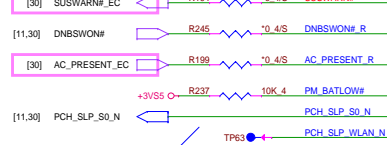
Input to PCH M cannot float. This pin forces an internal reset to the PCH.



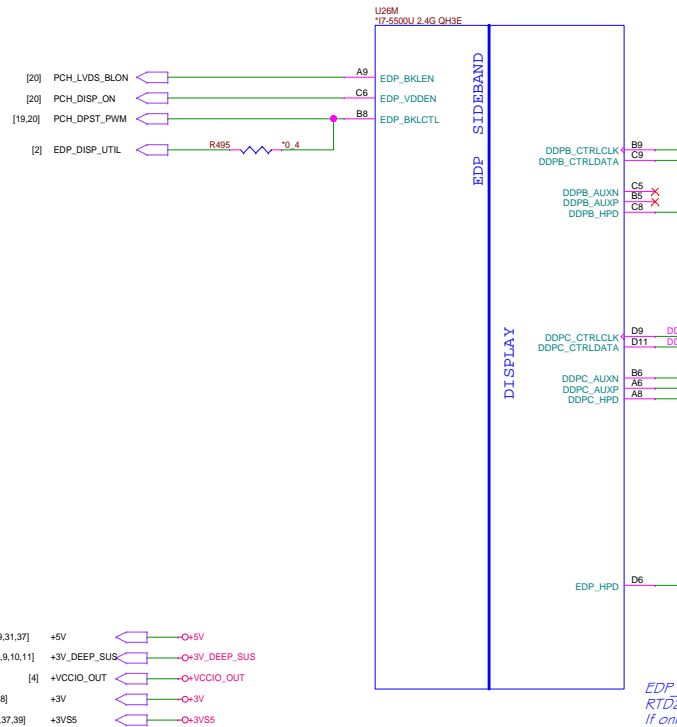
SUSPWRDNACK / SUSWARN#

This signal is Active-high and is driven low by the Intel(R) ME when it requires the PCH Suspend Well to be powered.

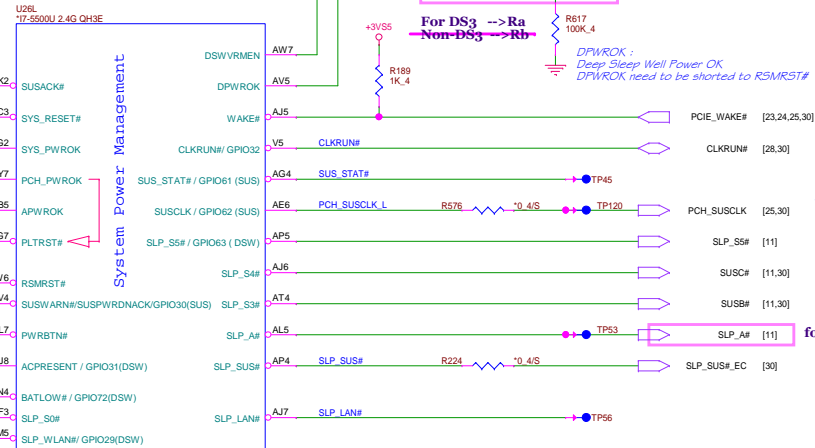
for DS3



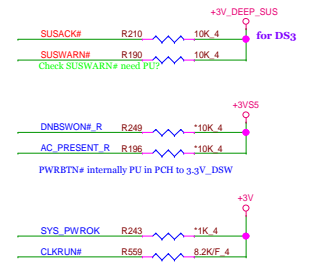
SLP_50# is a PCH signal which indicates the system is in the S0ix State. SLP_50# stays high in Sx and during Sx entry/exit. This signal will be low during low power state.



System Power Management



PCH Pull-high/low(CLG)

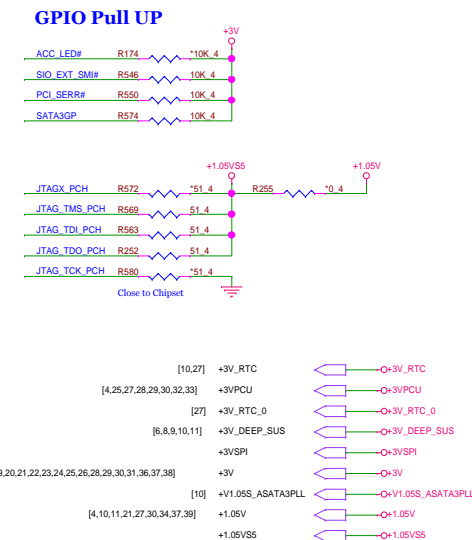


EDP_HPDI need pull down via 100KΩ, so combine with RTD2136 pin-1 DP_HPDI pull down resistor. If only for eDP panel, EDP_HPDI must stuff one 100KΩ.

Reserve EDP_HPDI opposites circuit!



Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0/GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden							
GSPi0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table><tr><th>GPIO#</th><th>Boot Location</th></tr><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPi(Default)</td></tr></table>	GPIO#	Boot Location	1	LPC	0	SPi(Default)	
GPIO#	Boot Location									
1	LPC									
0	SPi(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up							



Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)

Cardreader

WLAN

LAN

GPU

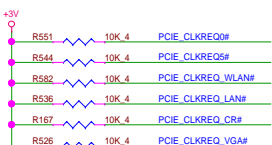
Card

WE CAN

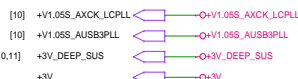
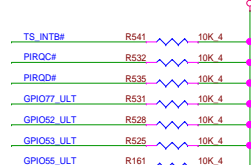
LAN

VCA

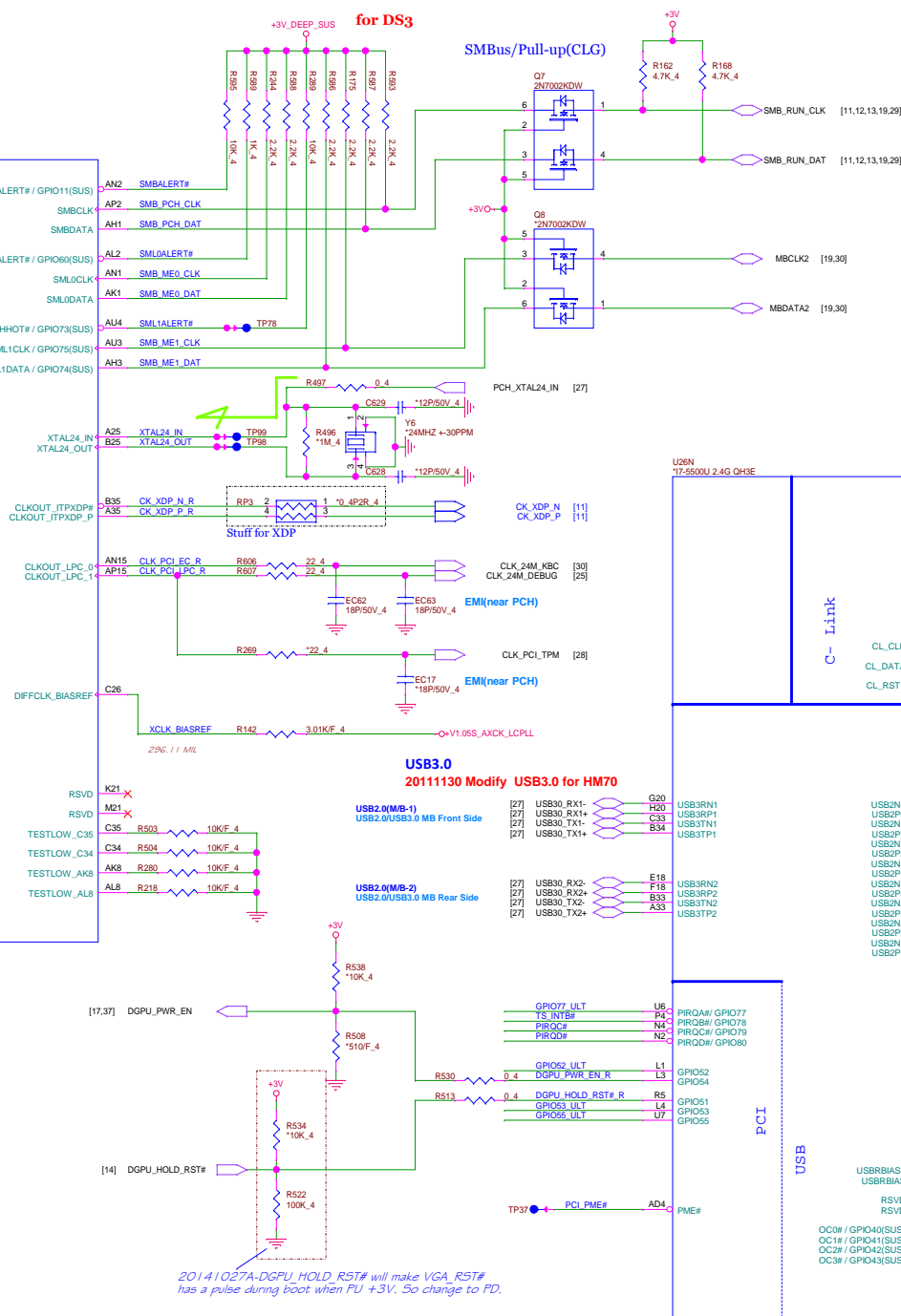
CLK_REQ/Strap Pin(CLG)



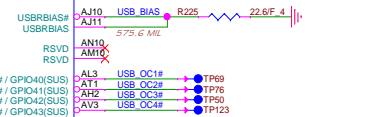
PCI/USBOC# Pull-up(CLG)



CLOCK SIGNALS

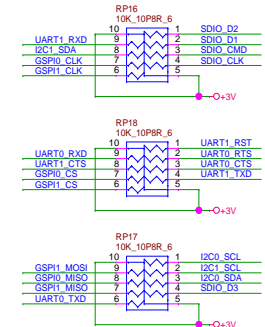
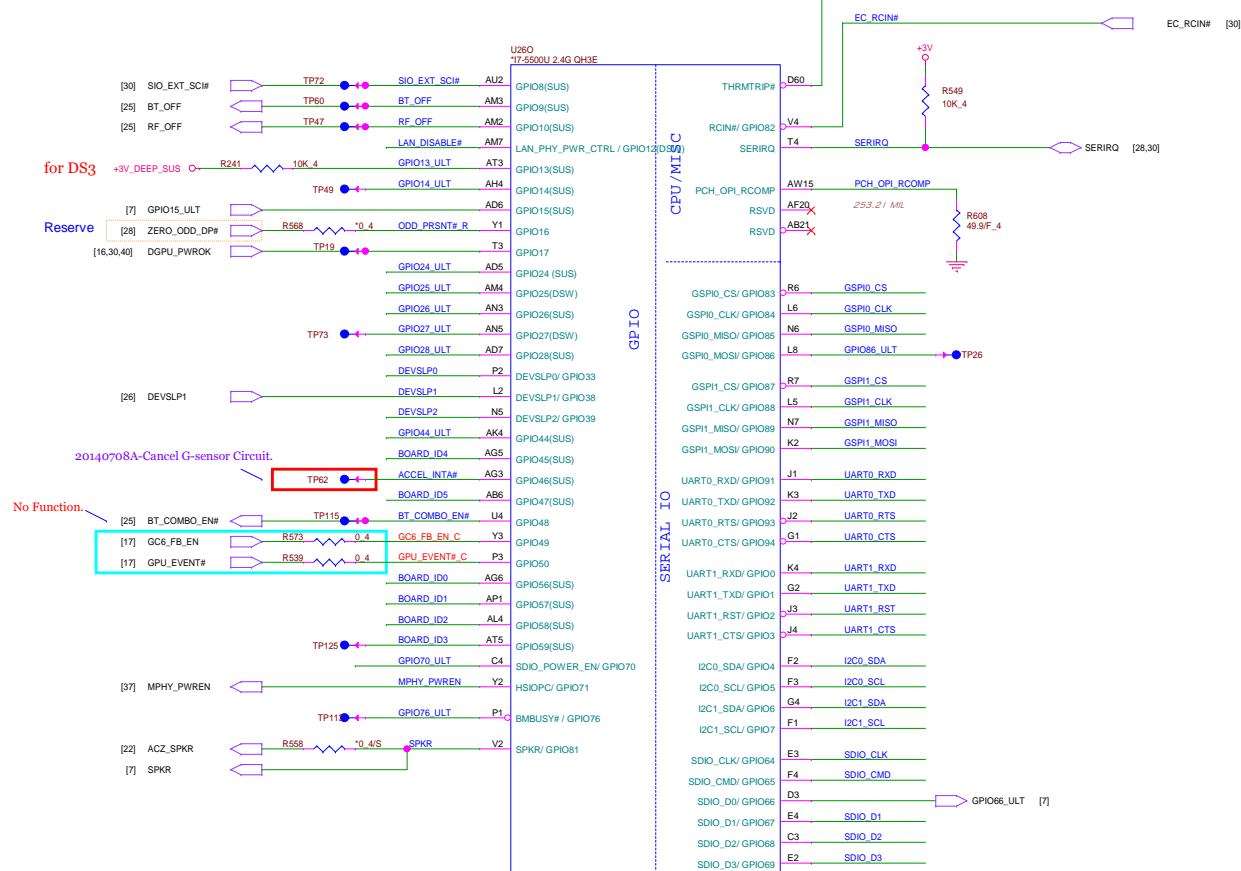


TIE TRACES TOGETHER CLOSE TO PINS WITH LENGTH TO RESISTOR

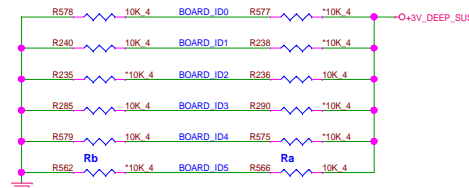
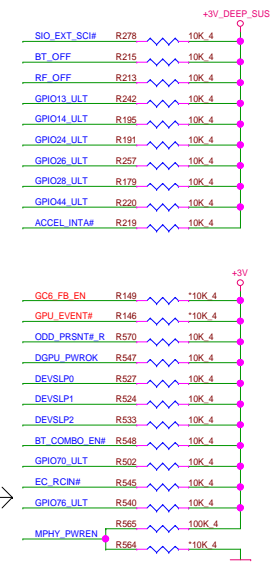


Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)

Haswell (GPIO)



GPIO Pull-up/Pull-down (CLG)



Model	BOARD_ID0 GPIO56 TWB : 0 JWV : 1	BOARD_ID1 GPIO57 No Define	BOARD_ID2 GPIO58 N16V : 0 N16S : 1	BOARD_ID3 GPIO59 No Define	BOARD_ID4 GPIO45 No Define	BOARD_ID5 GPIO47 UMA : 0 dGPU : 1
TWB + UMA	0	0	0	0	0	0
TWB + dGPU + N16S	0	0	1	0	0	1
TWB + dGPU + N16V	0	0	0	0	0	1
JWV + UMA	1	0	0	0	0	0
JWV + dGPU + N16S	1	0	1	0	0	1
JWV + dGPU + N16V	1	0	0	0	0	1

20141008A-BIOS request for SVID, N16S-GT need PU GPIO58 (BOARD_ID2).

[6,7,8,10,11,12,13,14,16,17,19,20,21,22,23,24,25,26,28,29,30,31,36,37,38]

[6,10,11,22,25,26,31,33,34,37,38]

[2,4,11,36] +V1.05S_VCCST

[6,7,8,10,11] +3V_DEEP_SUS

+3V

[6,10,11,22,25,26,31,33,34,37,38] +3V55

+V1.05S_VCCST

+3V_DEEP_SUS

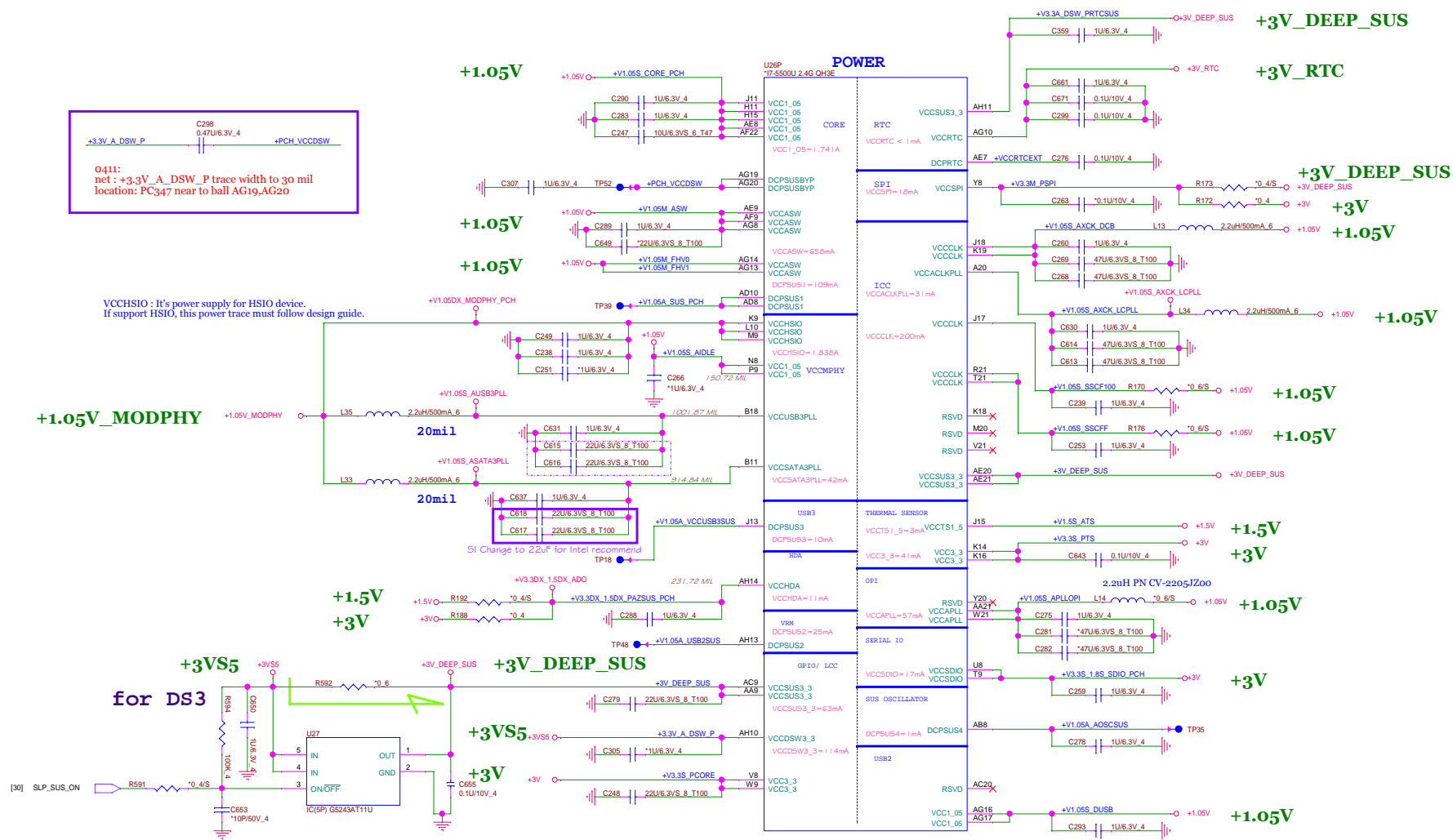
+3V













+3V55

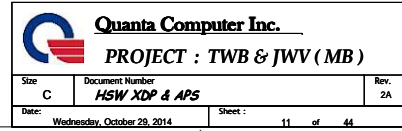
Quanta Computer Inc.
PROJECT : TWB & JWV (MB)

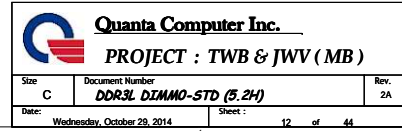
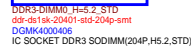
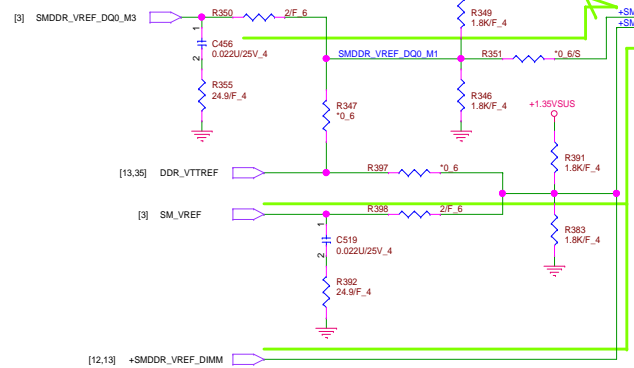
Size C	Document Number ULT 8/9 (GPIO/MISC)	Rev. 2A
Date: Wednesday, October 29, 2014	Sheet : 9 of 44	

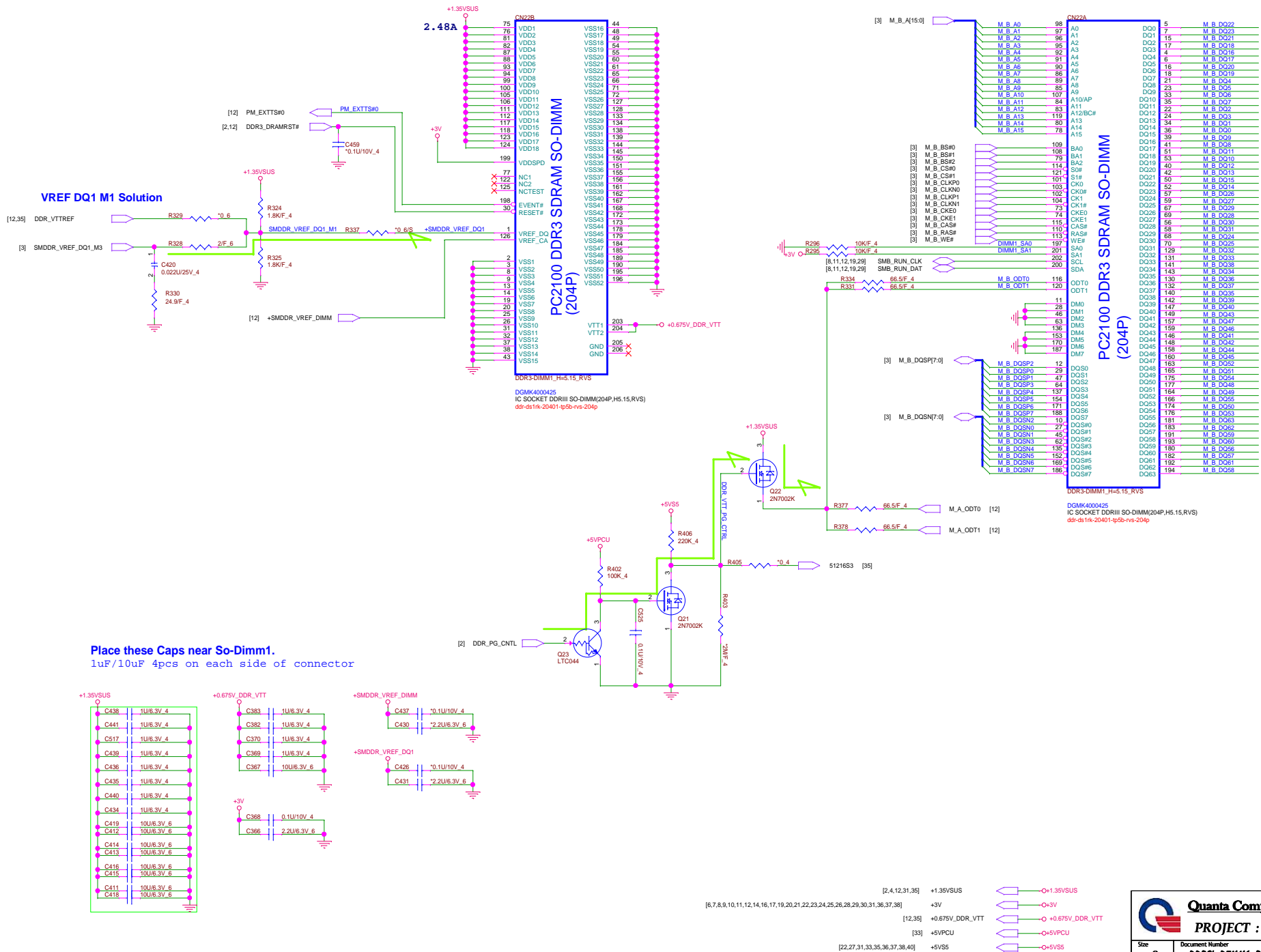
Lynx Point-LP Platform Controller Hub
(HDA,JTAG,SATA)(POWER)

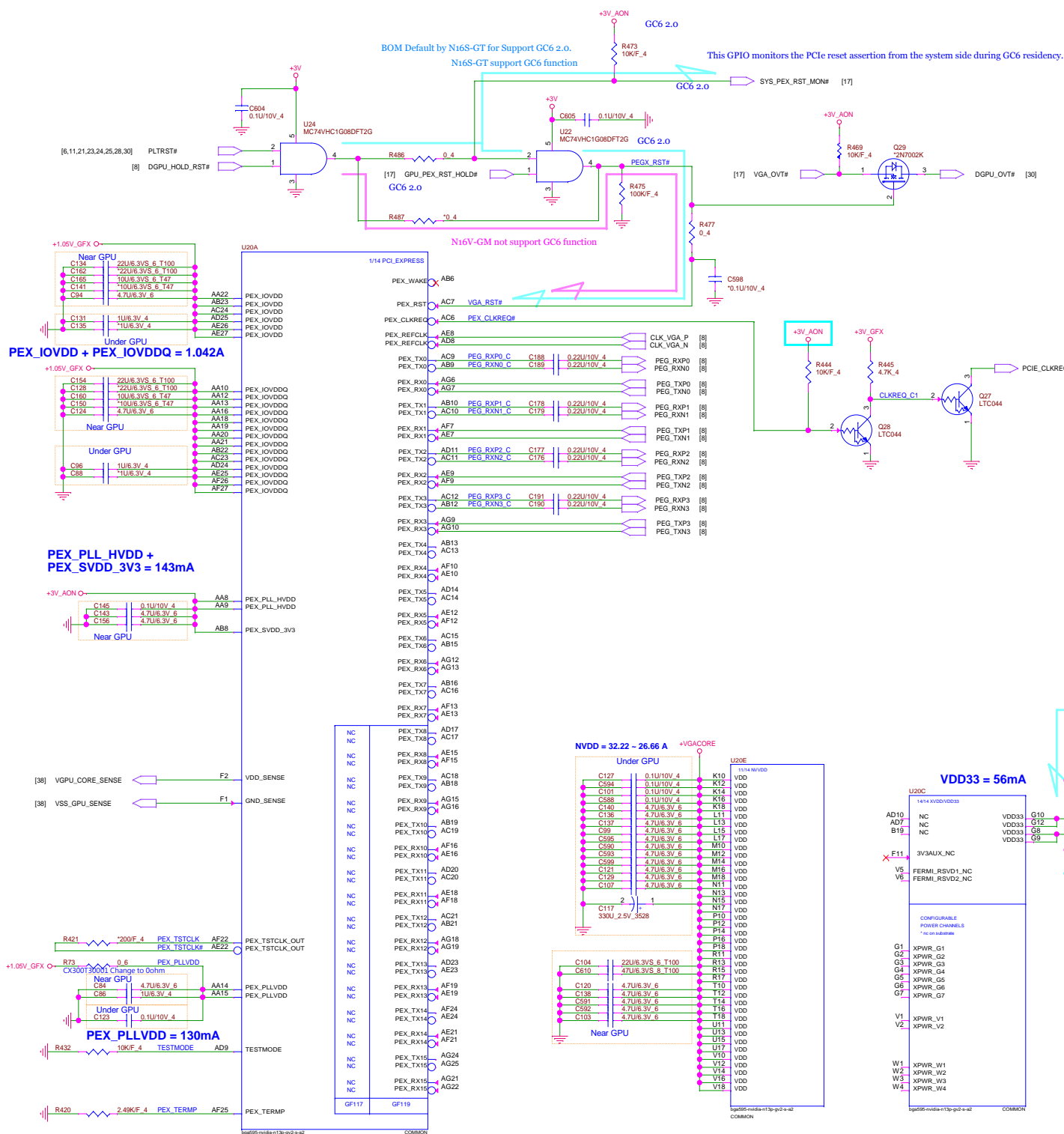


- | | | | |
|---------------------------------|----------------------|---|-----------------------|
| [37] | +V1.05D_X_MODPHY_PCH |  | →+V1.05D_X_MODPHY_PCH |
| [37] | +1.05V_MODPHY |  | →+1.05V_MODPHY |
| [8] | +V1.05S_AXCK_LCPLL |  | →+V1.05S_AXCK_LCPLL |
| | +V3.3D_X_1.5D_X_ADO |  | →+V3.3D_X_1.5D_X_ADO |
| [8] | +V1.05S_AUSB3PLL |  | →+V1.05S_AUSB3PLL |
| [7] | +V1.05S_ASATAS3PLL |  | →+V1.05S_ASATAS3PLL |
| [6,7,8,9,11] | +3V_DEEP_SUS |  | →+3V_DEEP_SUS |
| | [22,25,26,34] |  | →+1.5V |
| 5,26,28,29,30,31,36,37,38] | +3V |  | →+3V |
| 5,9,11,22,25,28,31,33,34,37,39] | +3VS5 |  | →+3VS5 |
| | [7,27] |  | →+3V_RTC |
| [4,7,11,21,27,30,34,37,39] | +1.05V |  | →+1.05V |

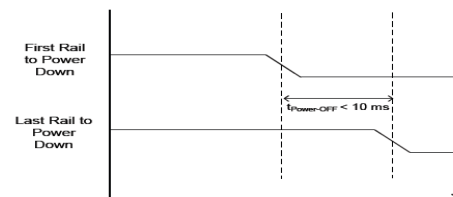
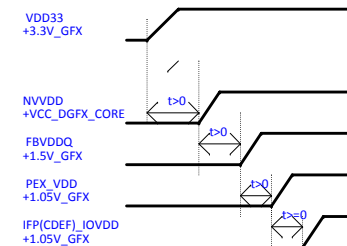




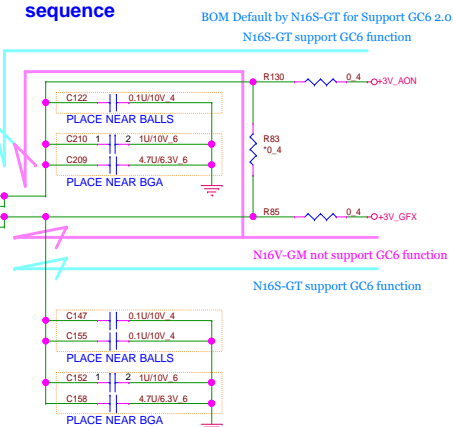


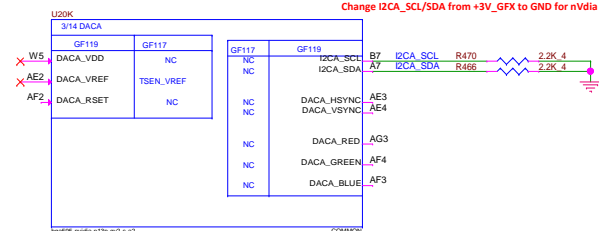
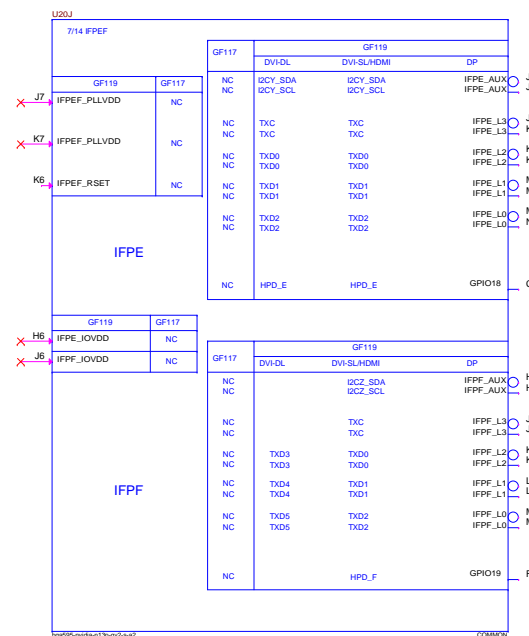


Power up sequence

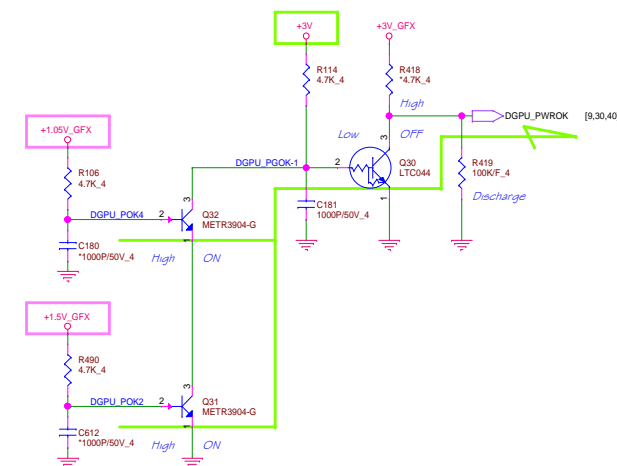
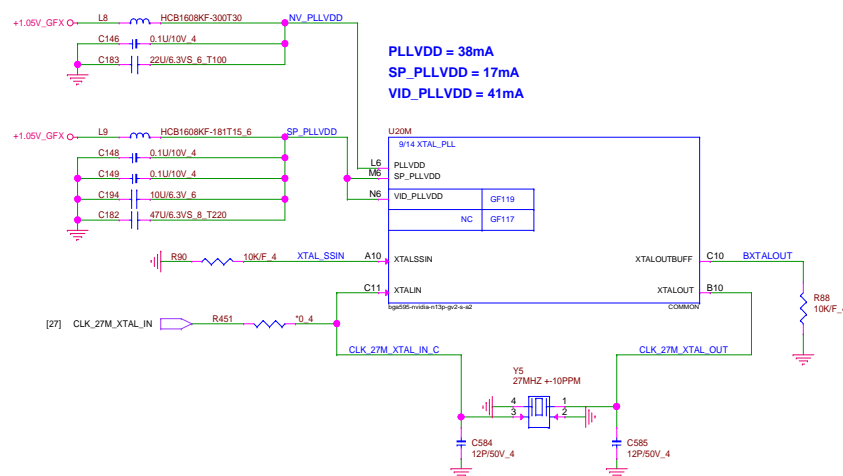
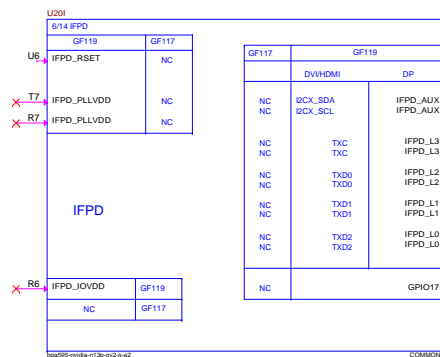
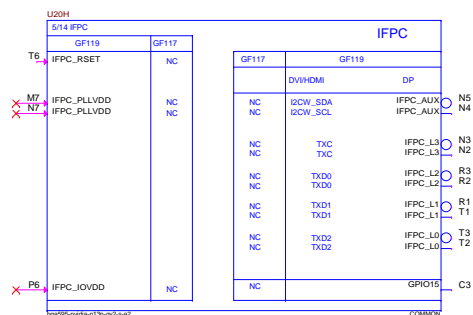


Power down sequence

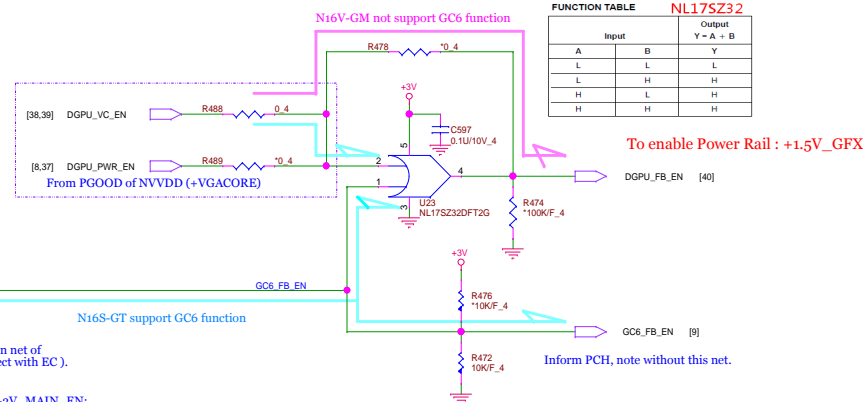
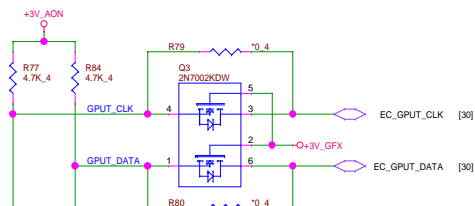
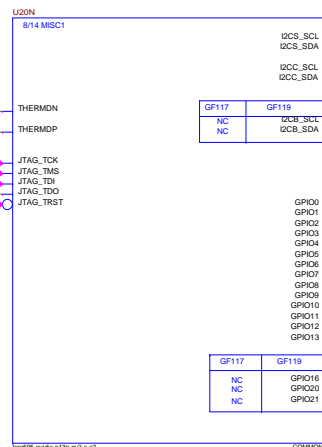
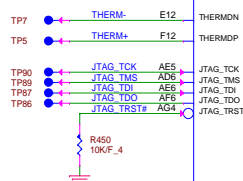




GPI/O	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



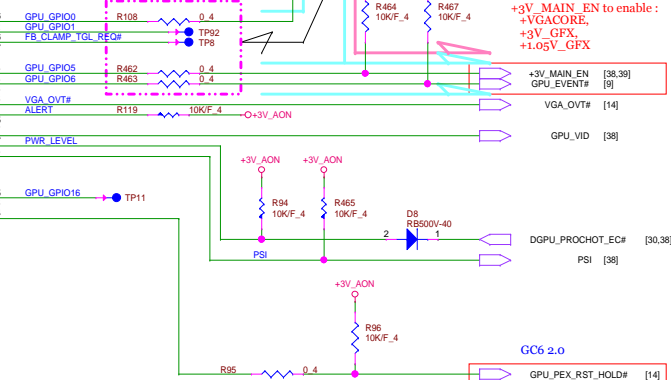
BOM Default by N16S-GT		N16S-GT GC6 (O)	N16V-GM GC6 (X)
GPU_GPIO0	R108	STUFF	NO STUFF
GPU_GPIO5	R462	STUFF	NO STUFF
	R464	STUFF	STUFF
GPU_GPIO6	R463	STUFF	NO STUFF
	R467	STUFF	STUFF

20140811A-Remove GC6 V1.0 function net of
FB CLAMP TGL REQ# EC (connect with EC).

+3V_MAIN_EN:
W/ Support GC6 enable by GPU_GPIO5.
W/O support GC6 enable by +3V_AON.

+3V_MAIN_EN to enable :
+VGACORE,
+3V_GFX,
+1.05V GFX

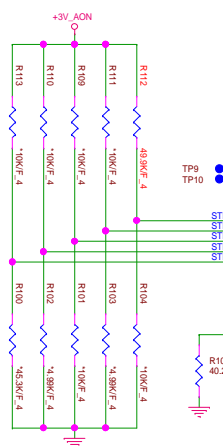
Inform CPU.



GC6 2.0

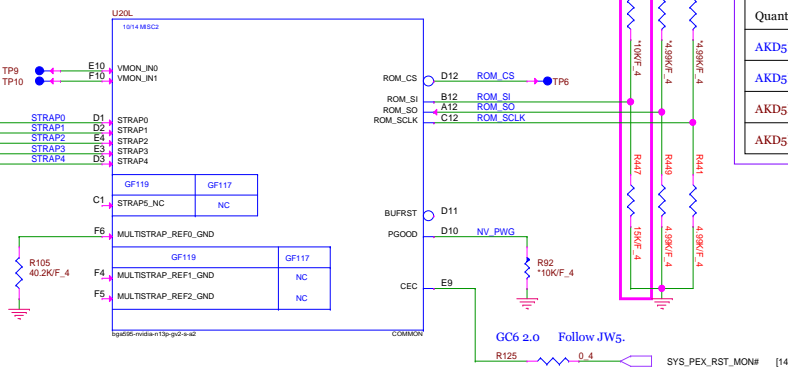
CPU BEY. RST. HOLD# [44]

ROM_S1 (Memory strap setting)
BOM Default by 15KΩ PD for Samsung K4W4G1646D-BC1A for N16S-GT.
N16S-GT



N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 110010

DEL VID pin for NVD request



Quanta P/N	VRAM	Part Description	Value	Resistor
AKD5PGWTW05	Hynix	H5TC4G63AFR-11C	0000	PD 4.99KΩ (R447)
AKD5PGWT500	Samsung	K4W4G1646D-BC1A	0010	PD 15KΩ (R447)

N16V-GM

Quanta P/N	VRAM	Part Description	Value	Resistor
AKD5PGWTW05	Hynix	H5TG4C63AFR-11C	0010	PD 15.0KΩ (R447)
AKD5PGWT500	Samsung	K4W4G1646D-BC1A	0100	PD 24.9KΩ (R447)
AKD5MZDTW04	Hynix	H5TG2G63FFR-11C	0011	PD 20.0KΩ (R447)
AKD5MGST511	Samsung	K4W2G1646Q-BC1A	0110	PD 34.8KΩ (R447)

BOM Default by N16S-GT	Location	N16S-GT GC6 (O)	N16V-GM GC6 (X)
ROM_SI	R446 R447	RVL	RVL
ROM_SO	R448 R449	PD 4.99KΩ	PU 4.99KΩ
ROM_SCLK	R440 R441	PD 4.99KΩ	PU 4.99KΩ
STRAP0	R112 R104	PU 49.9KΩ	PU 45.3KΩ
STRAP1	R111 R103	NU	PD 4.99KΩ
STRAP2	R109 R101	NU	PU 10KΩ
STRAP3	R110 R102	NU	PD 4.99KΩ
STRAP4	R113 R100	NU	PD 45.3KΩ

ROM_SI (Memory strap setting)

* Both for 940M (N16S-GT) & 920M (N16V-GM)

Following iWU VRAM...			
VRAM P/N		Vender	VRAM Size
AKD5PGWTW05	IC SDRAM(96P)H5TC4G63AFR-11C(FBGA)	Hynix	4G*4=16G=2G byte
AKD5PGWT500	IC SDRAM(96P)K4W4G1646D-BC1A(FBGA)	Samsung	4G*4=16G=2G byte

* Only for 920M (N16V-GM)

VRAM P/N	VRAM	VRAM Size
AKD5M2DTW04	Hynix	1C SDRAM(96P)H5TC2G63FFR-11C(FBGA)
AKD5MGST511	Samsung	1C SDRAM(96P)K4W2G1646Q-BC1A(FBGA)

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001 Ox1 Micron
15.0 kΩ	1010	0010 Ox2 Hynix
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100 Ox4 Samsung
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 3. N16S-GM/-GT/-LP DDR3 Recommended Memories

Memory Type	FBVDD/FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK/Grade/Min/A	Memory Data Cycle Minimum	Status
DDR3	1.5V/1.3V	128Mbit	Single Rank or Single Rank Stuffed for Dual Rank	Hynix	H5TC463F3R-11C	F-die	0x0	1000	N/A	Product candidate
				Samsung	K4J1128M16J2-093C-K	K-die	0x7	1000	1322	Product candidate
		256Mbit	Single Rank or Single Rank Stuffed for Dual Rank	Samsung	K4V261640-BC1A	B-die	0x8	1000	N/A	Product candidate
				Hynix	H5TC463F3R-11C	A-die	0x0	1000	N/A	Product candidate
				Samsung	K4J11250M16A-093C-E	E-die	0x1	1000	1322	Product candidate
				Samsung	K4V261640-BC1A	D-die	0x2	1000	N/A	Product candidate
			Dual Rank	Hynix	H5TC463F3R-11C	A-die	0x0	1000	N/A	Product candidate
				Samsung	K4J11250M16A-093C-E	E-die	0x1	1000	1322	Product candidate
				Samsung	K4V261640-BC1A	D-die	0x2	1000	N/A	Product candidate

N16V-GM DDR3 & DDR3L MEMORY RVL

Note: For H16V-GM, the maximum allowable memory case temperature is 85 °C.

Table 1. N16V-GM DDR3 Recommended Memories

Memory type	FBVDV/ FBVOC	Memory Density	Configuration	Vendor	Manufacturer Part Number	Dig. Clock	Strap	Memory Speed CK (Data rate)	Memory Data Rate	Status
DDR3	1.5V/ 1.5V	128MiB	Single Rank or Single Rank Dual Rank For Stacking	Hynix	HTJ4G303FFR-1E	F-die	On3	1000	N/A	Product candidate
				Micron	HTJ14G303FFR-093G-IC	F-die	On3	1000	1322	Product candidate
				Samsung	K4G401646G-BC1A	A-die	On3	1000	1322	Product candidate
	1.5V/ 1.5V	256MiB	Single Rank or Single Rank Dual Rank For Stacking	Hynix	HTJ24G646G-093G-IC	F-die	On3	1000	1322	Product candidate
				Hynix	HT57C4G303FFR-1E	A-die	On2	1000	N/A	Product candidate
				Samsung	K4W401646G-BC1A	A-die	On4	1000	N/A	Product candidate

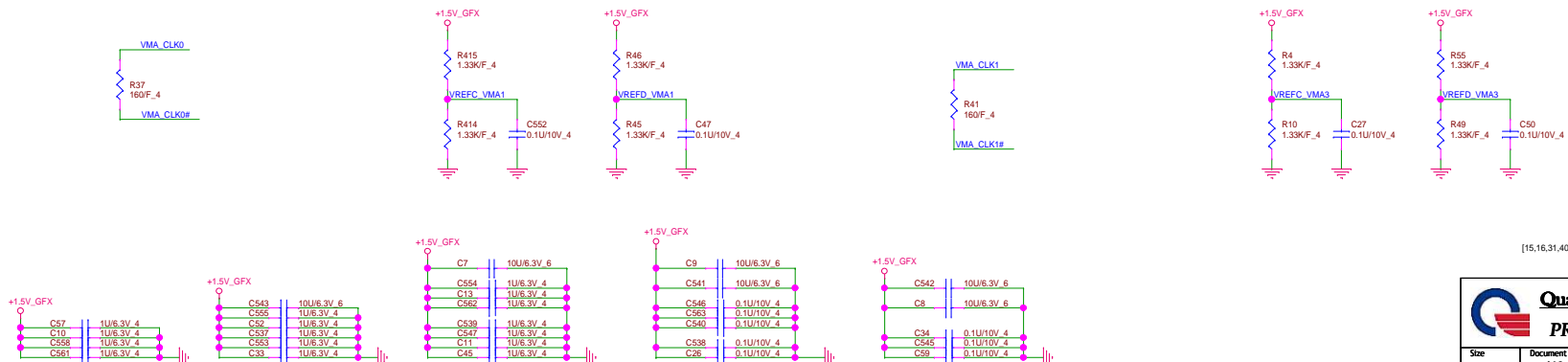
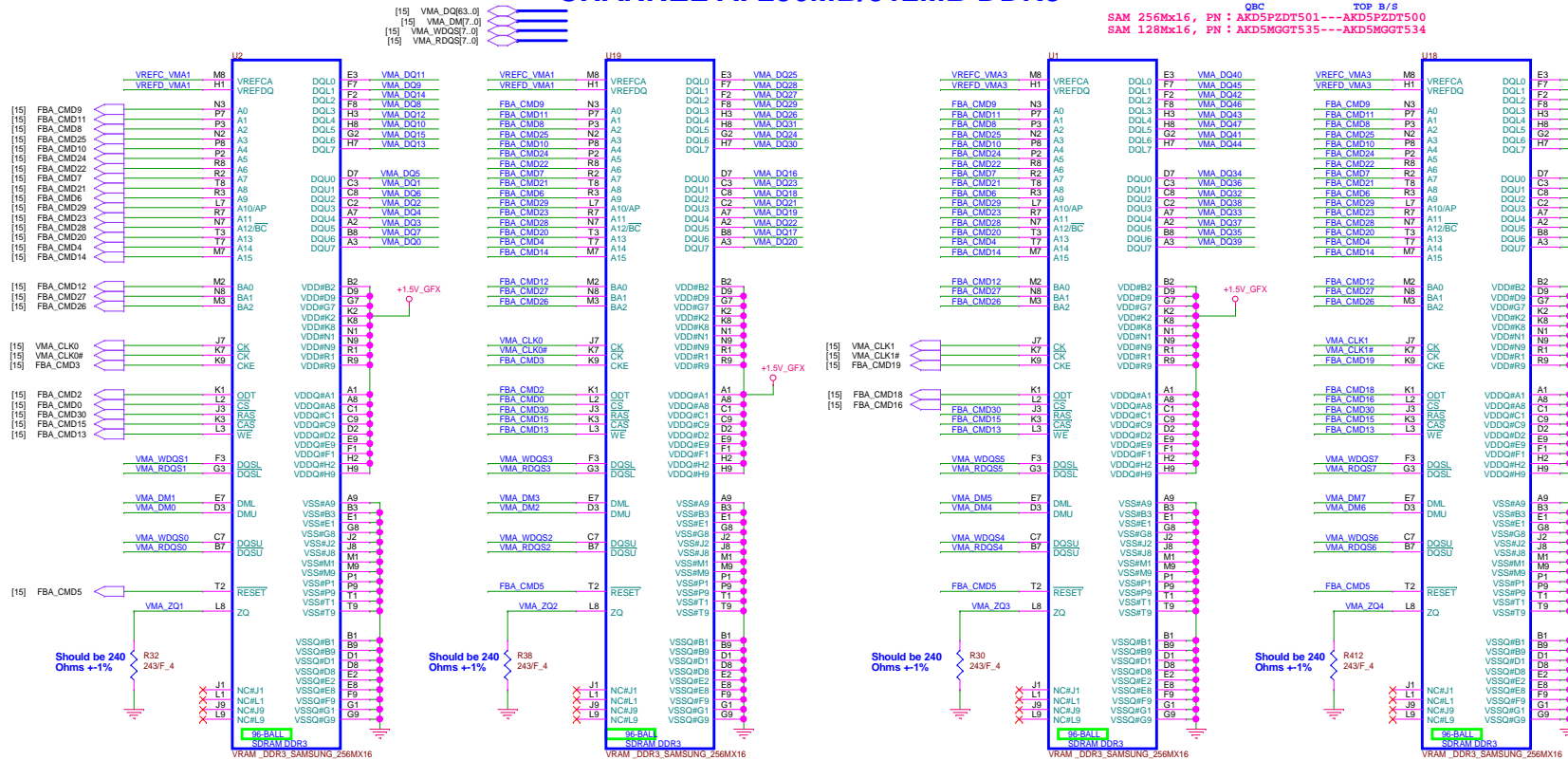
**Quanta Computer Inc.**

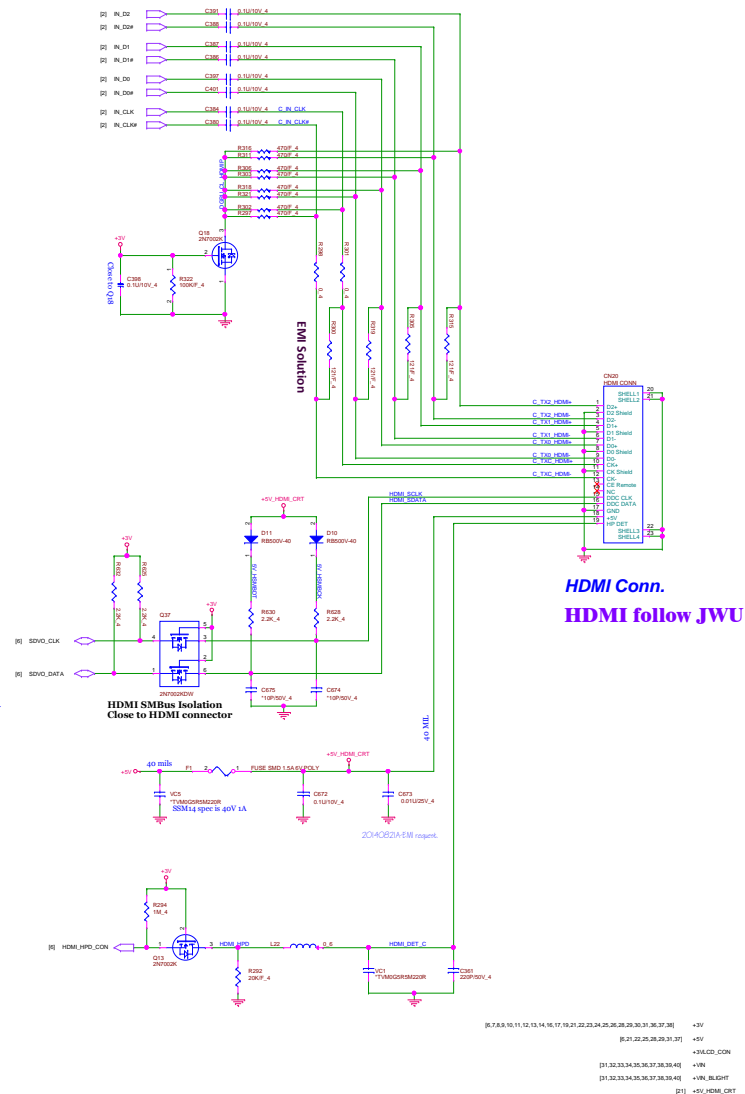
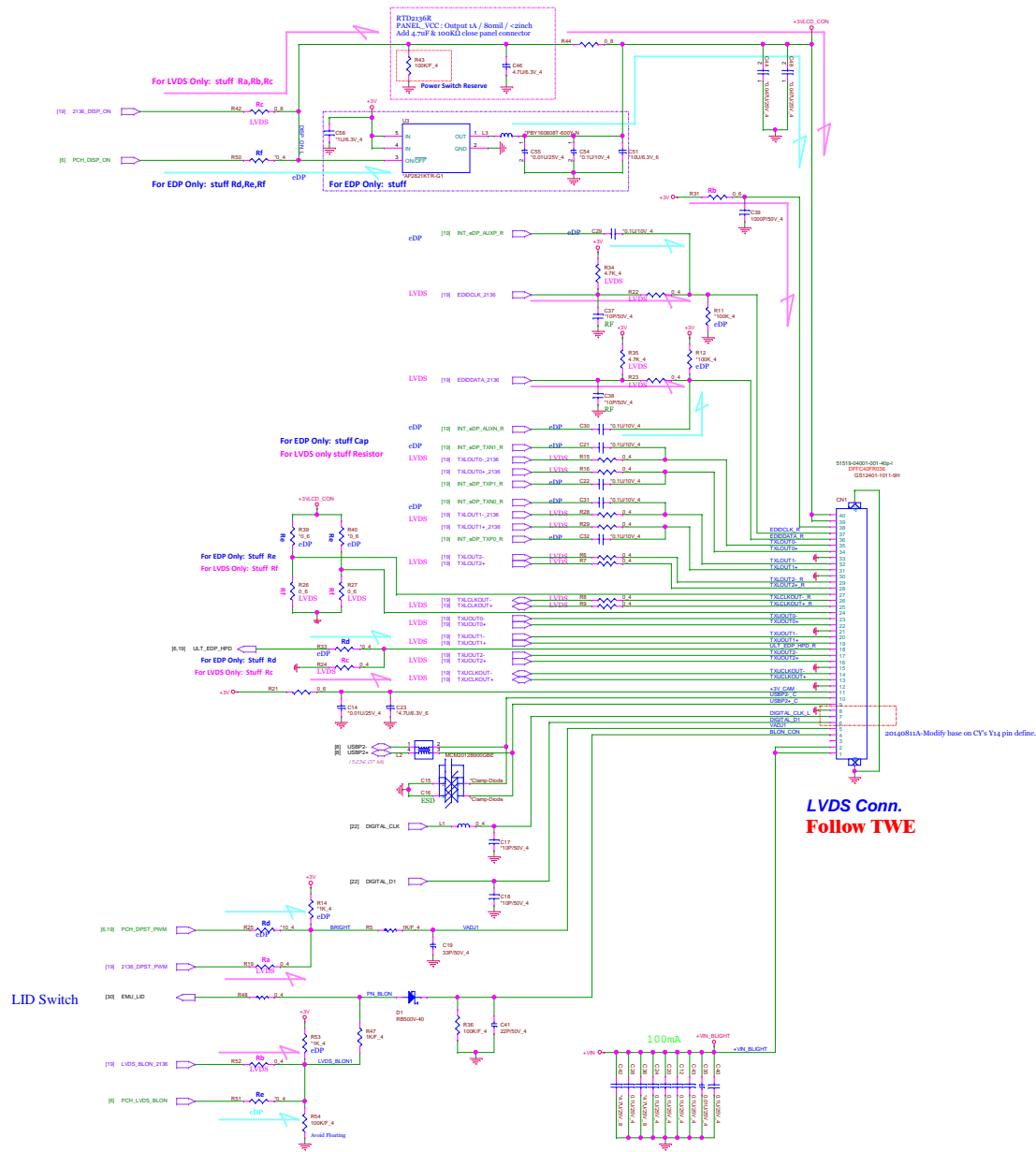
PROJECT : TWB & JWV (MB)

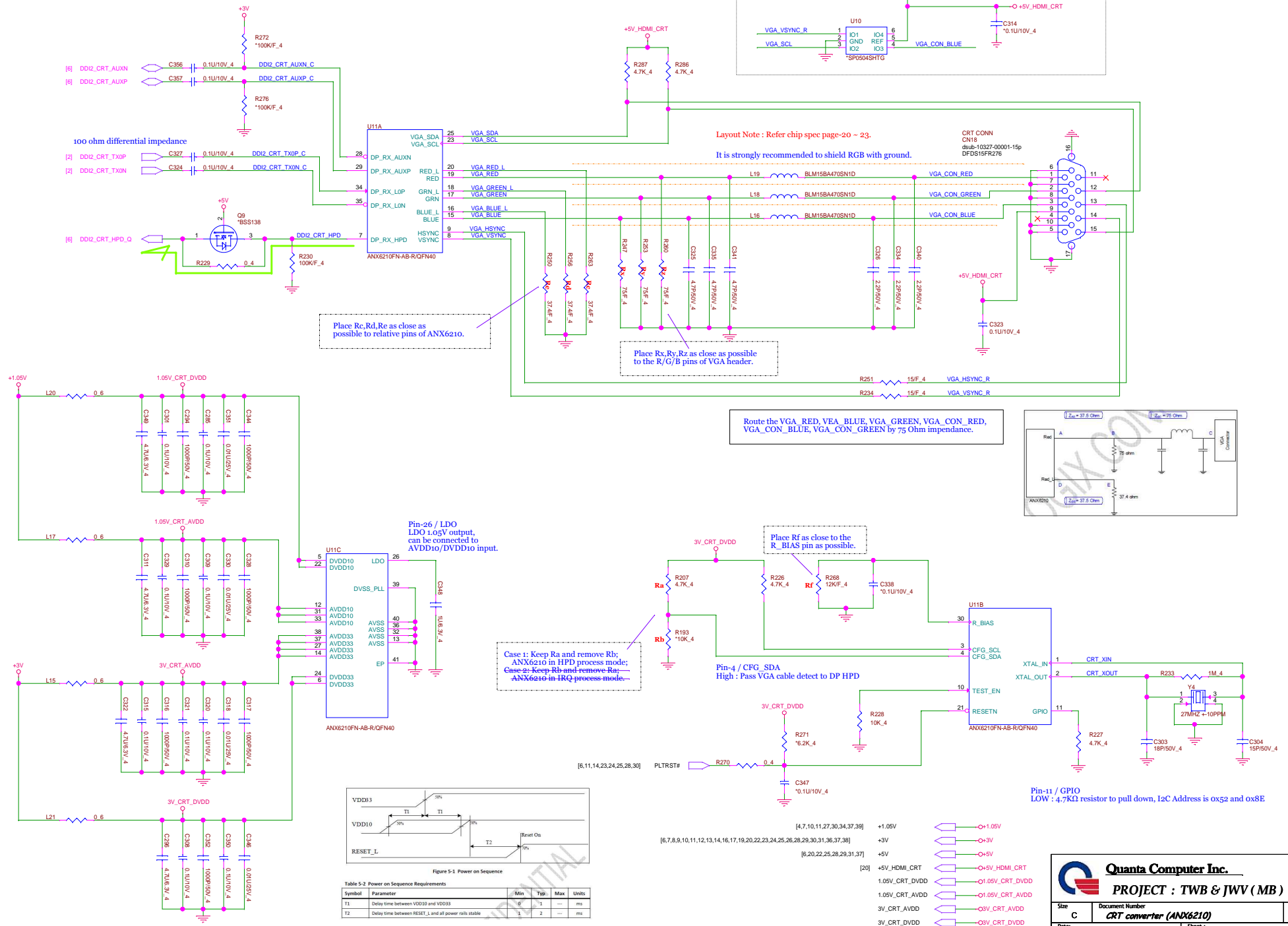
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Date: Wednesday, October 29, 2014	Sheet : 17 of 44

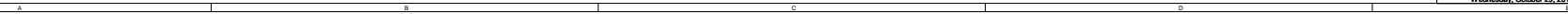
CHANNEL A: 256MB/512MB DDR3

HYU 256Mx16, PN : AKD5PGWTW08---AKD5PGWTW07
 HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02
 QBC
 SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500
 SAM 128Mx16, PN : AKD5MGDT535---AKD5MGDT534









9. Power Sequence

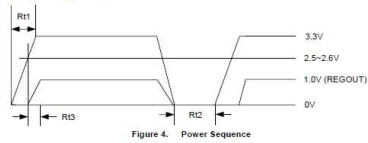
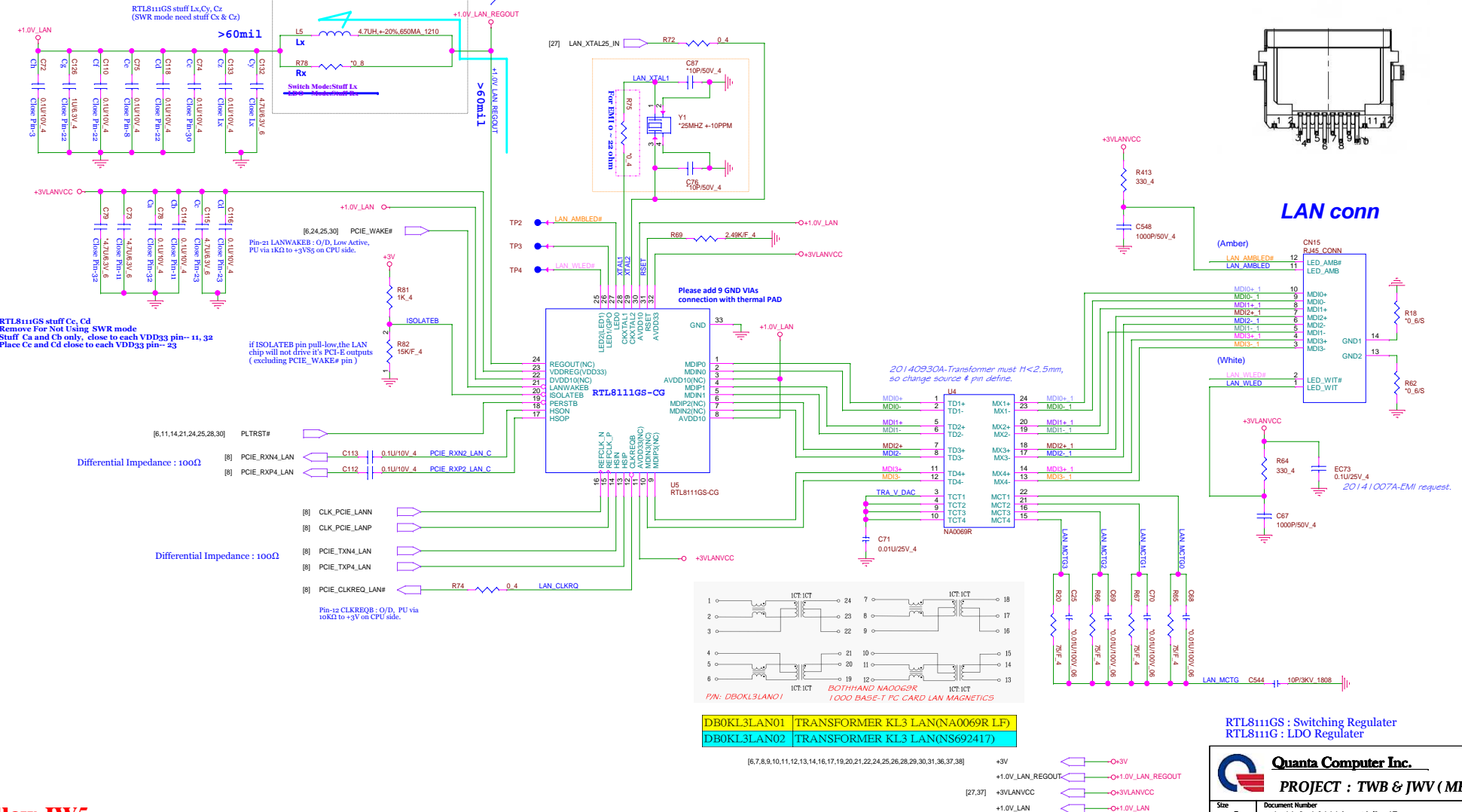


Table 16. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
R1	3.3V Rise Time	0.5	-	100	ms
R2	3.3V Off Time	50	-	-	ms
R3	1.0V (REGOUT) Settle Time	-	-	15	ms

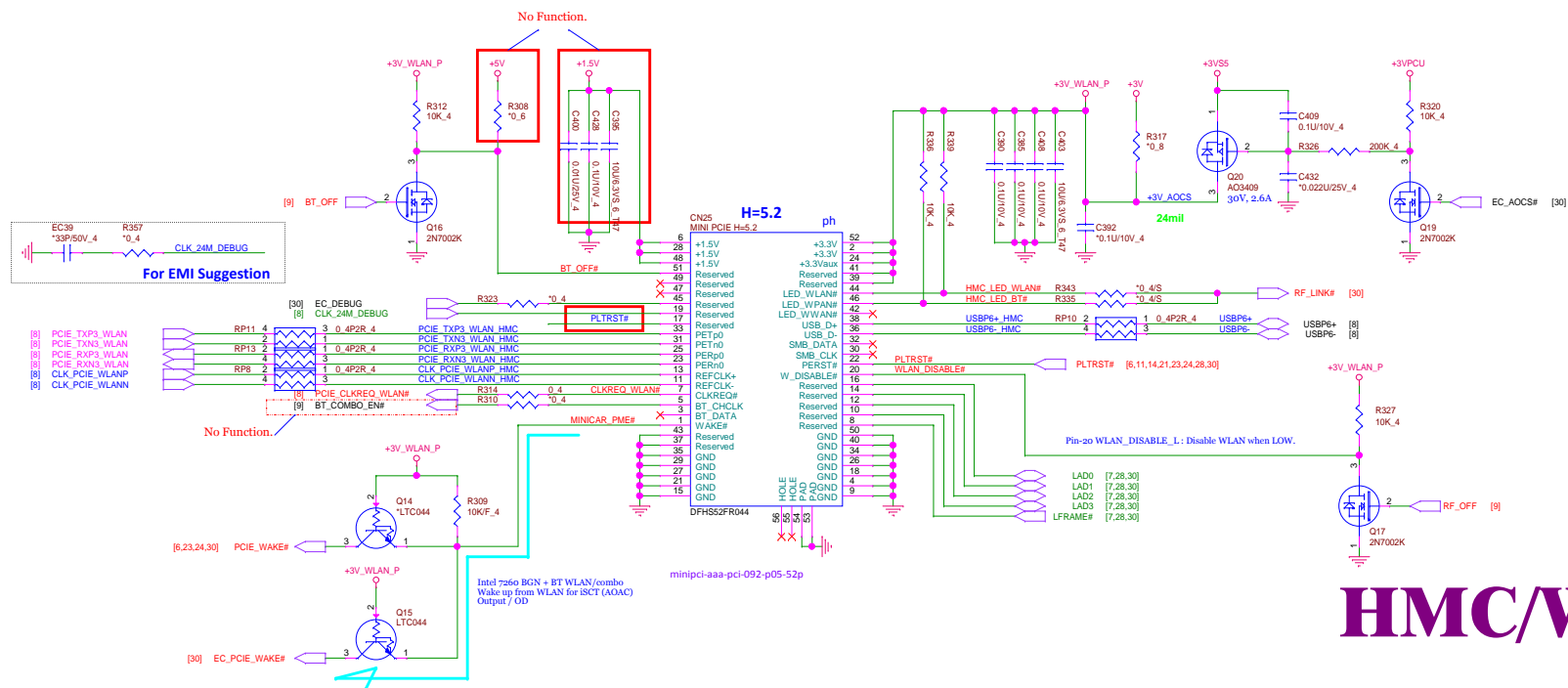
Note: See the following section for power sequence requirements.

Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3,8,22,30
Place Cg & Ch close to each VDD10 pin22



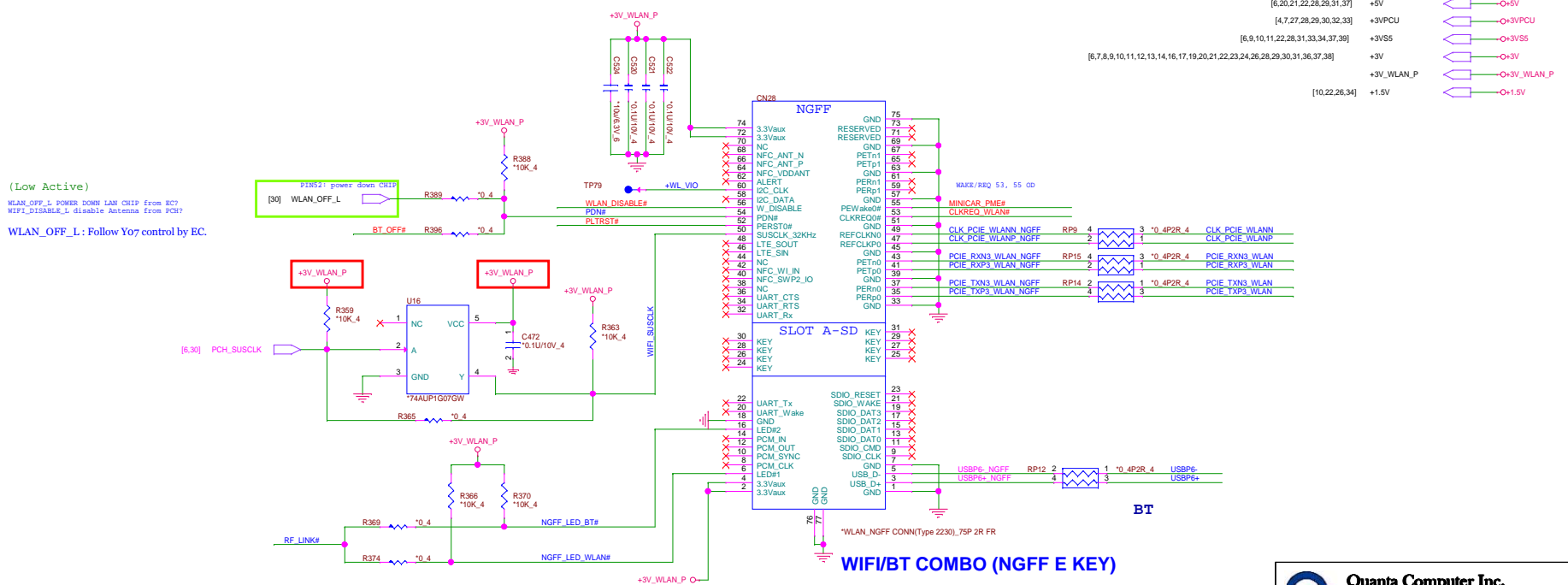


PIN-15	SP1	SD_D1	---	I/O	SD Data 1 (SD_D1)
PIN-16	SP2	SD_Do	MS_D1	I/O	SD Data 0 (SD_Do)
PIN-17	SP3	SD_CLK	MS_Do	I/O	SD Clock signal (SD_CLK)
PIN-19	SP4	SD_CMD	MS_D2	I/O	SD CMD signal (SD_CMD)
PIN-20	SP5	SD_D3	MS_D3	I/O	SD Data 3 (SD_D3)
PIN-21	SP6	SD_D2	MS_CLK	I/O	SD Data 2 (SD_D2)
PIN-29	SP7	SD_WP	MS_BS	I	SD Write Protect signal
PIN-30	SD_CD#	SD_CD#	---	I	SD Card Detection signal



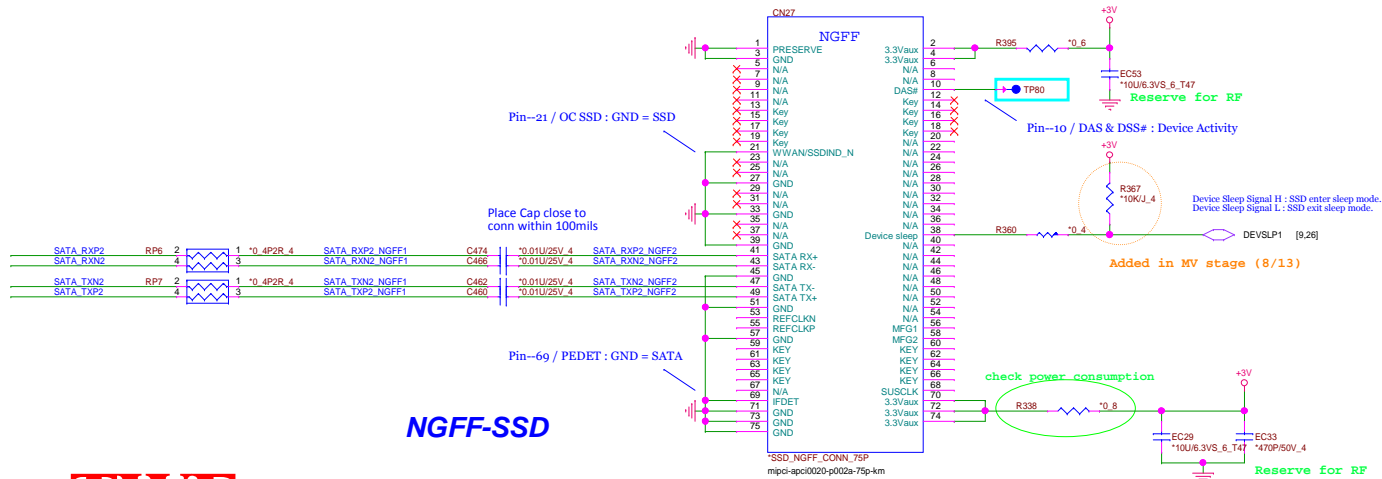
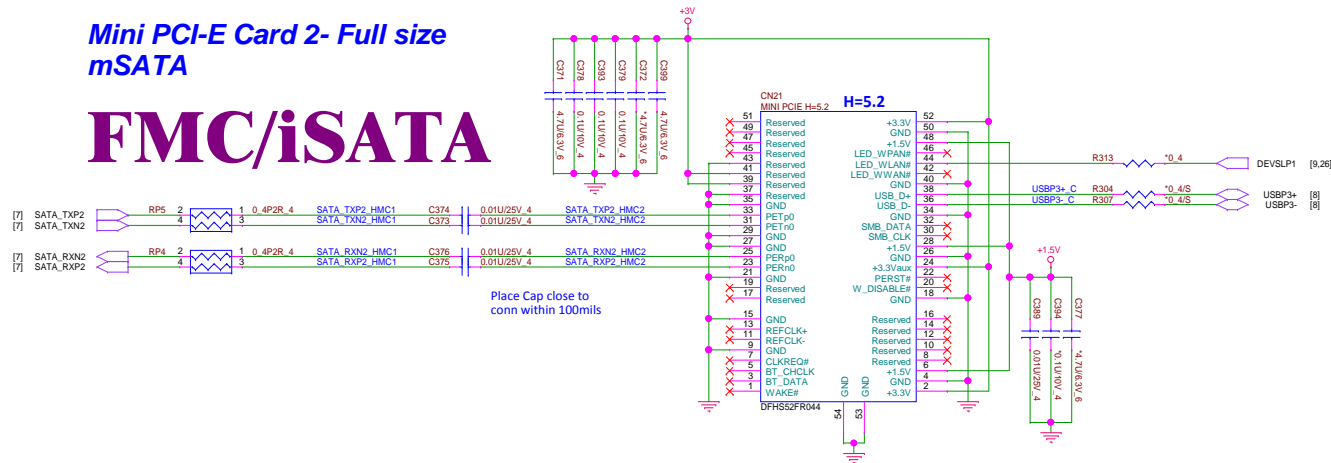
HMC/WLAN

Support Wake Function(Reserve)



Mini PCI-E Card 2- Full size
mSATA

FMC/iSATA



NGFF-SSD

Follow TWE
2280/2242

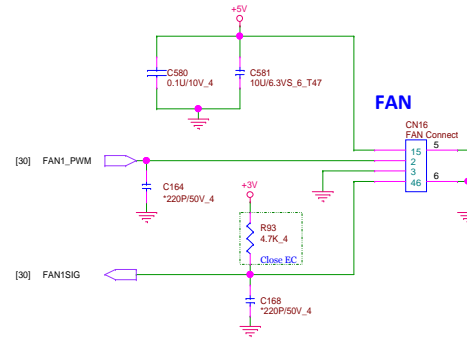
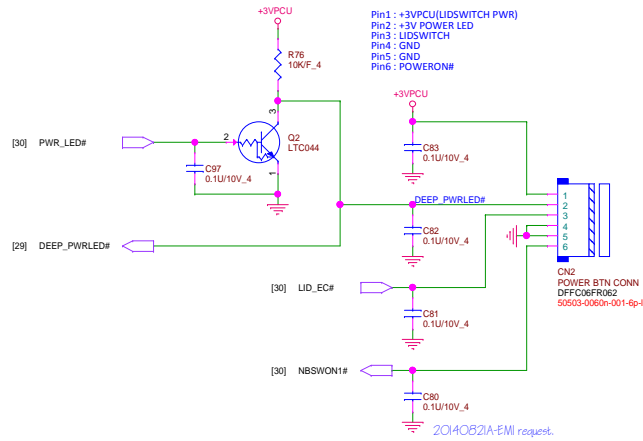
20140808-Change P/N & FP, must confirm pin define again.

mipci-apci0018-p002a-75p-kb

Input Voltage	Parameter	32GB	64GB	128GB	256GB	512GB
5V ± 5%	SATA 6Gb/s host interface					
	Read [mW]	NA	2,600	2,700	2,800	TBD
	Write [mW]	NA	2,200	3,350	4,800	TBD
3.3V ± 5%	Read [mW]	2,200	2,450	2,650	2,650	NA
	Write [mW]	2,100	2,150	3,400	4,500	NA

Table 3-3: SanDisk SSD X110 Average Max Power Consumption

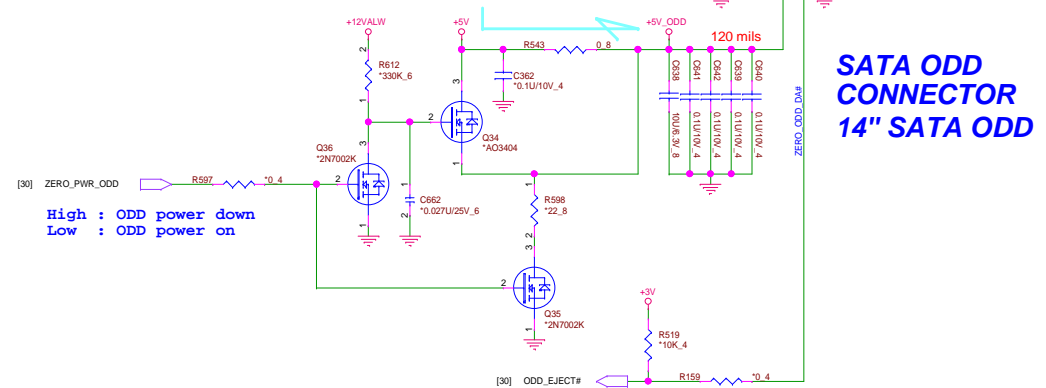
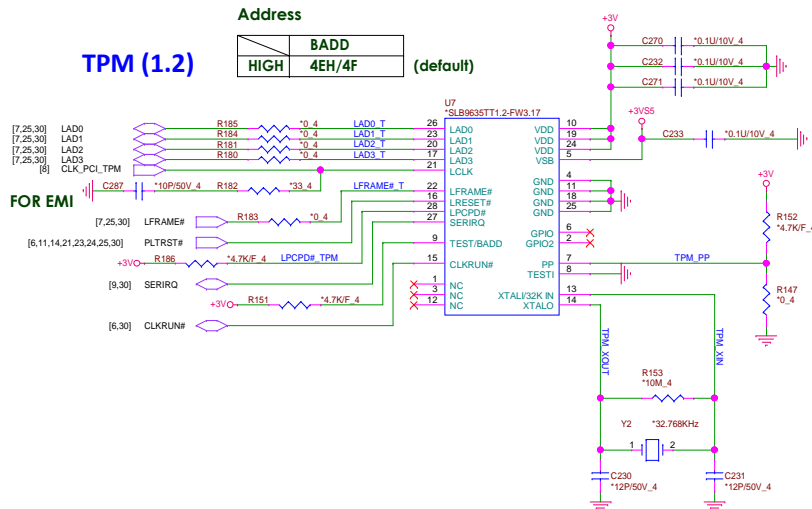
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

[illegible]

Address

	BADD
HIGH	4EH/4F

(default)

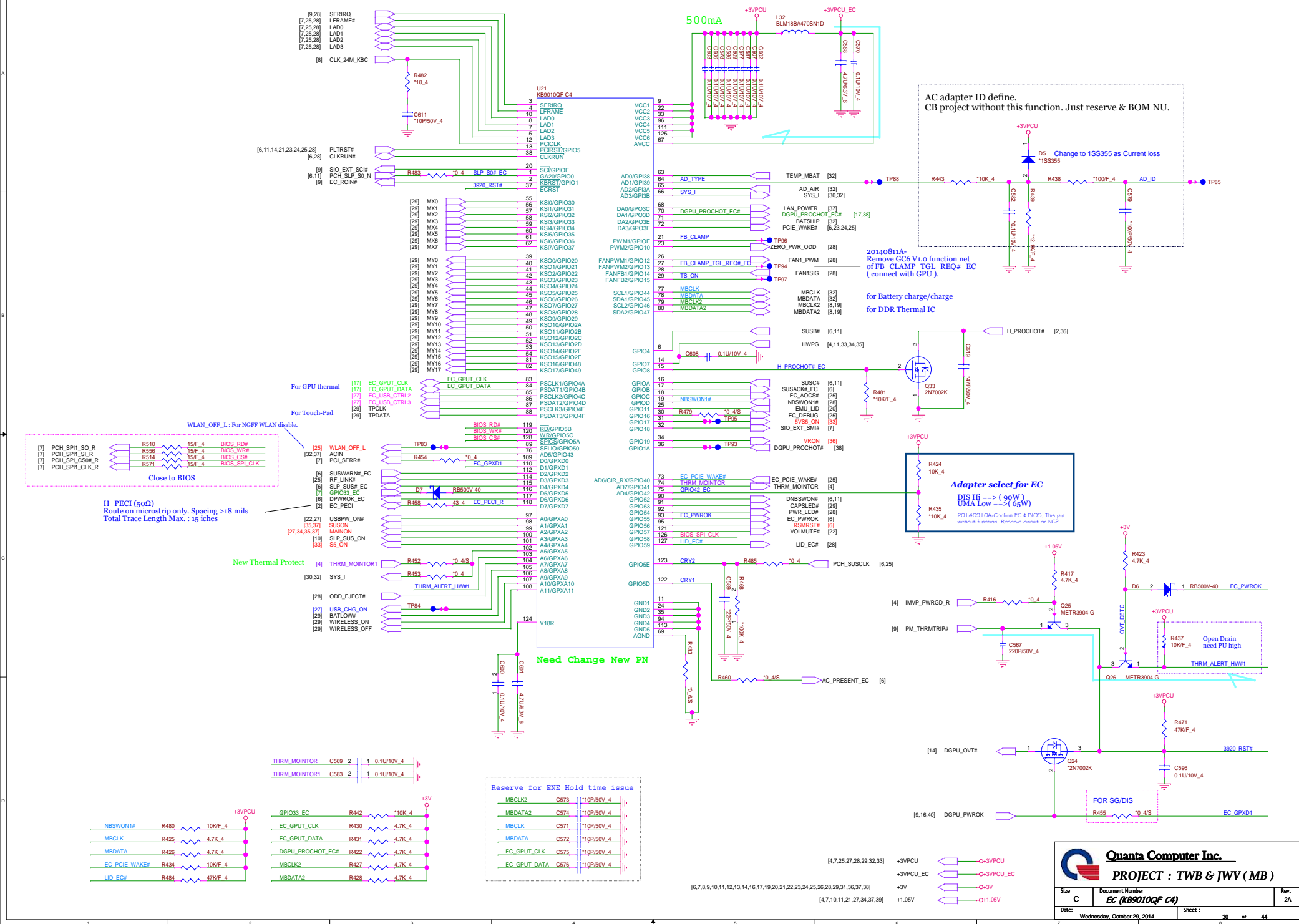


**SATA ODD
CONNECTOR
14" SATA ODD**

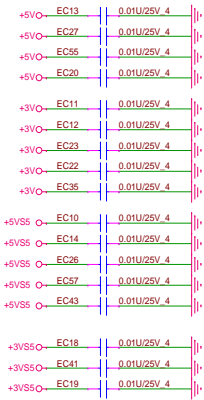
High : ODD power down
Low : ODD power on

[4,7,25,27,29,30,32,33]	+3VPCU		→+3VPCU
[5,26,29,30,31,36,37,38]	+3V		→+3V
[6,20,21,22,25,29,31,37]	+5V		→+5V
	+5V_ODD		→+5V_ODD
[37,39]	+12VALW		→+12VALW

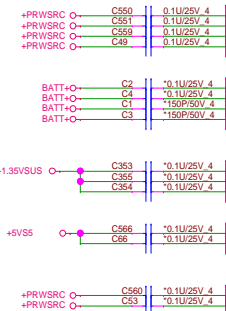
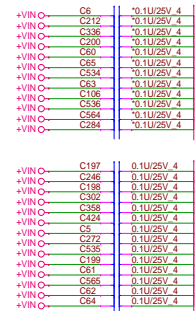
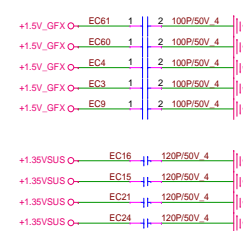
JWV remove G-sensor/Touch Screen function.



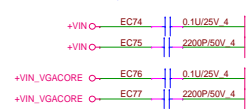
20140B29A-EMI request.



20140B26A-EMI request.



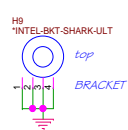
201400BA-EMI request for PV.



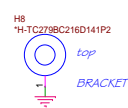
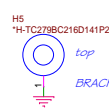
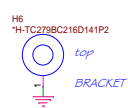
Hole

CPU BRACKET
P/N : FBUR6017010

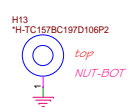
CPU Bracket

GPU BRACKET
P/N : FBR62021010

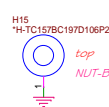
GPU Bracket

NGFF NUT
P/N : MBY01001010

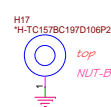
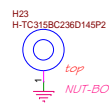
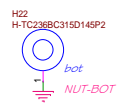
NGFF WLAN 2230



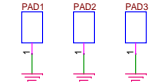
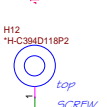
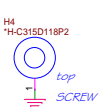
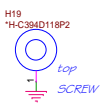
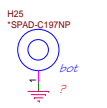
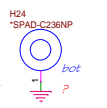
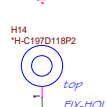
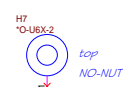
NGFF SSD 2240

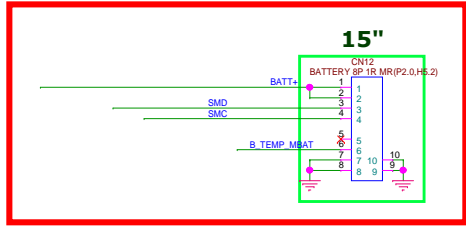


NGFF SSD 2280

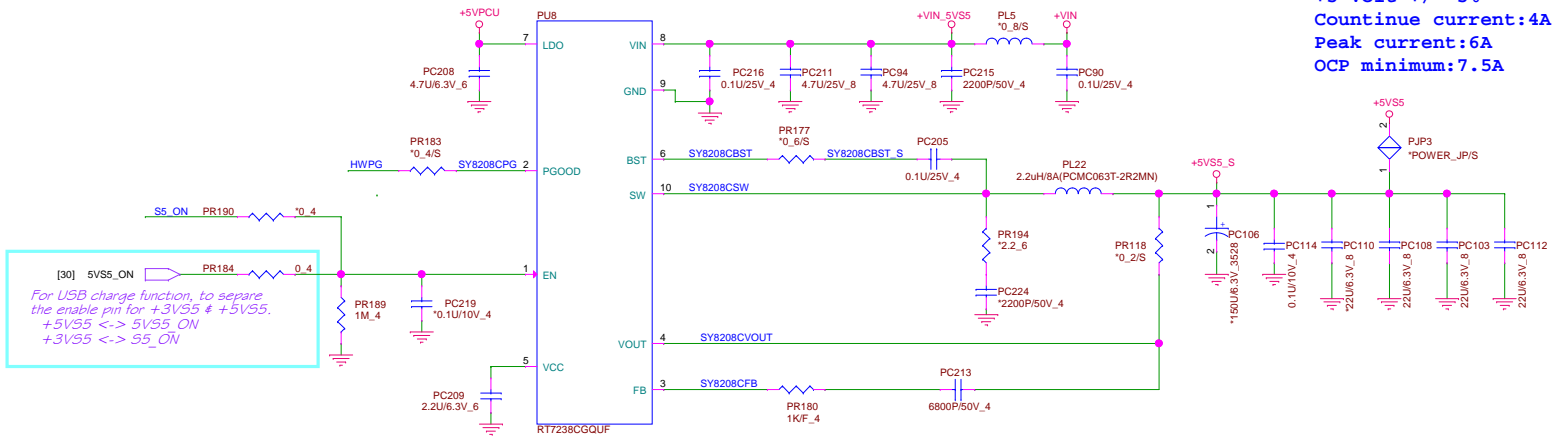
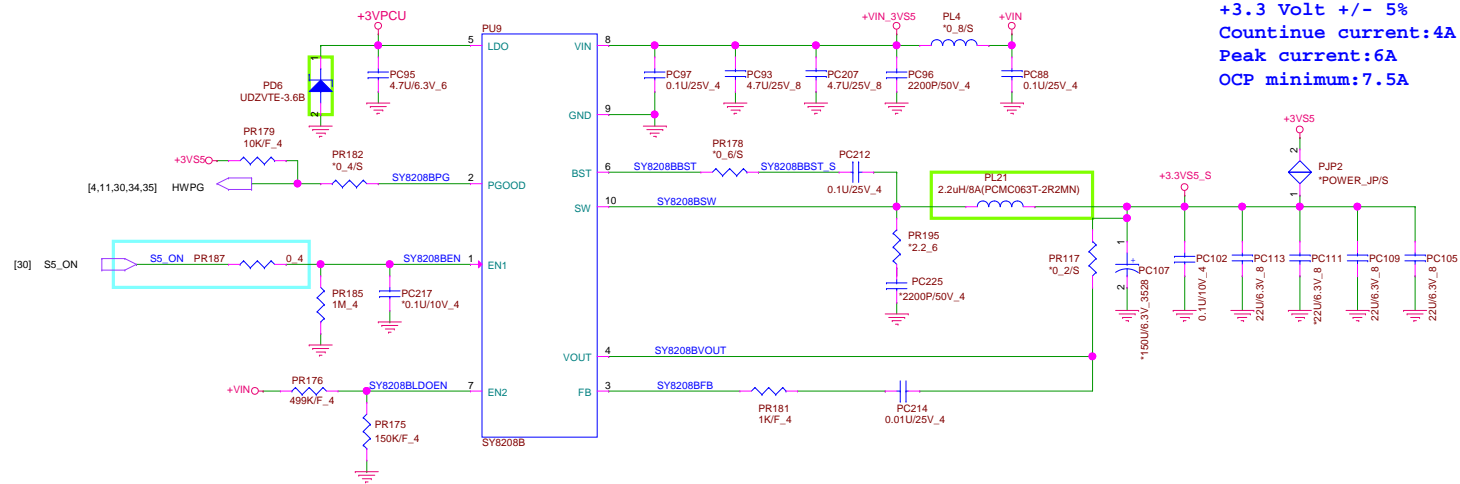
FAN NUT
P/N : MBFF4001010

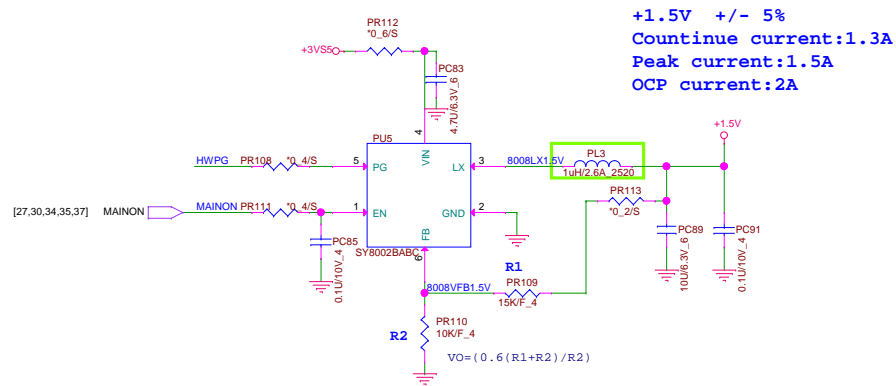
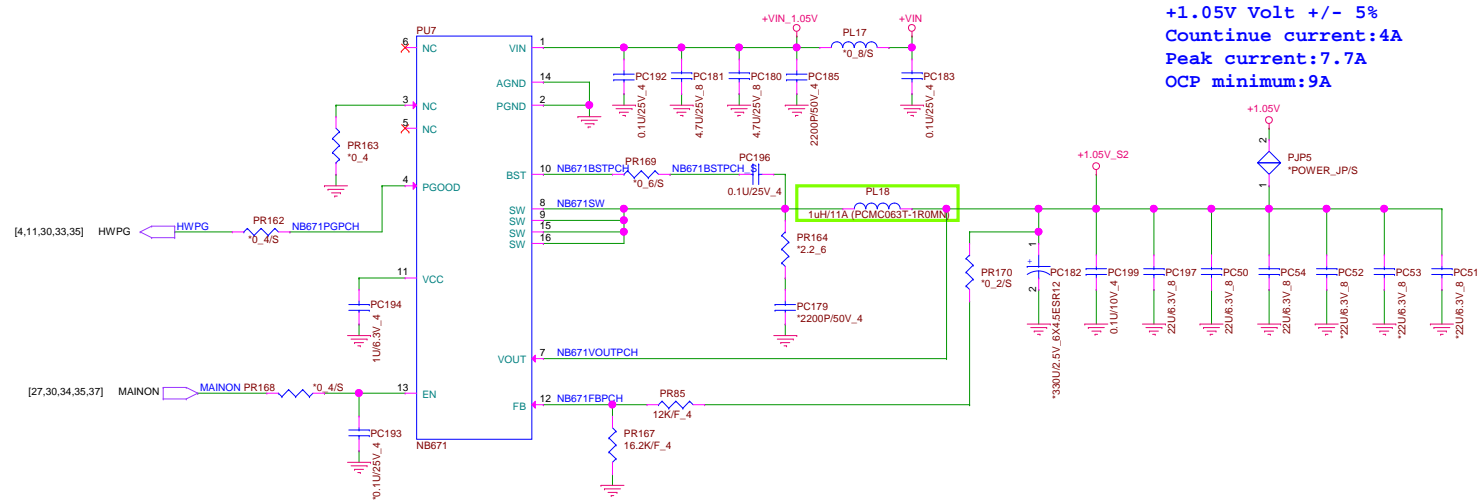
Thermal Module





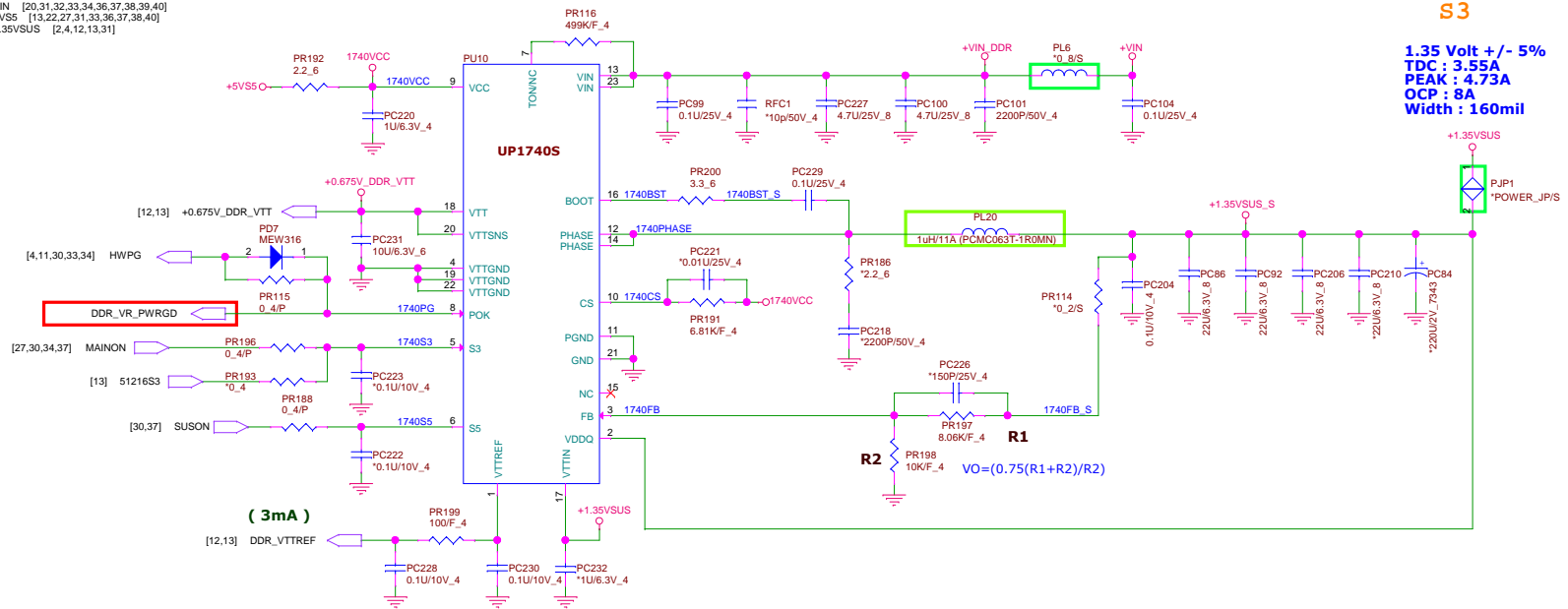
DC/DC +3VS5/+5VS5



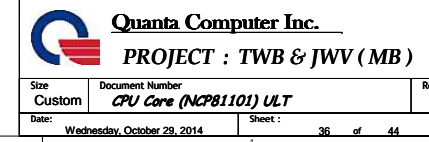


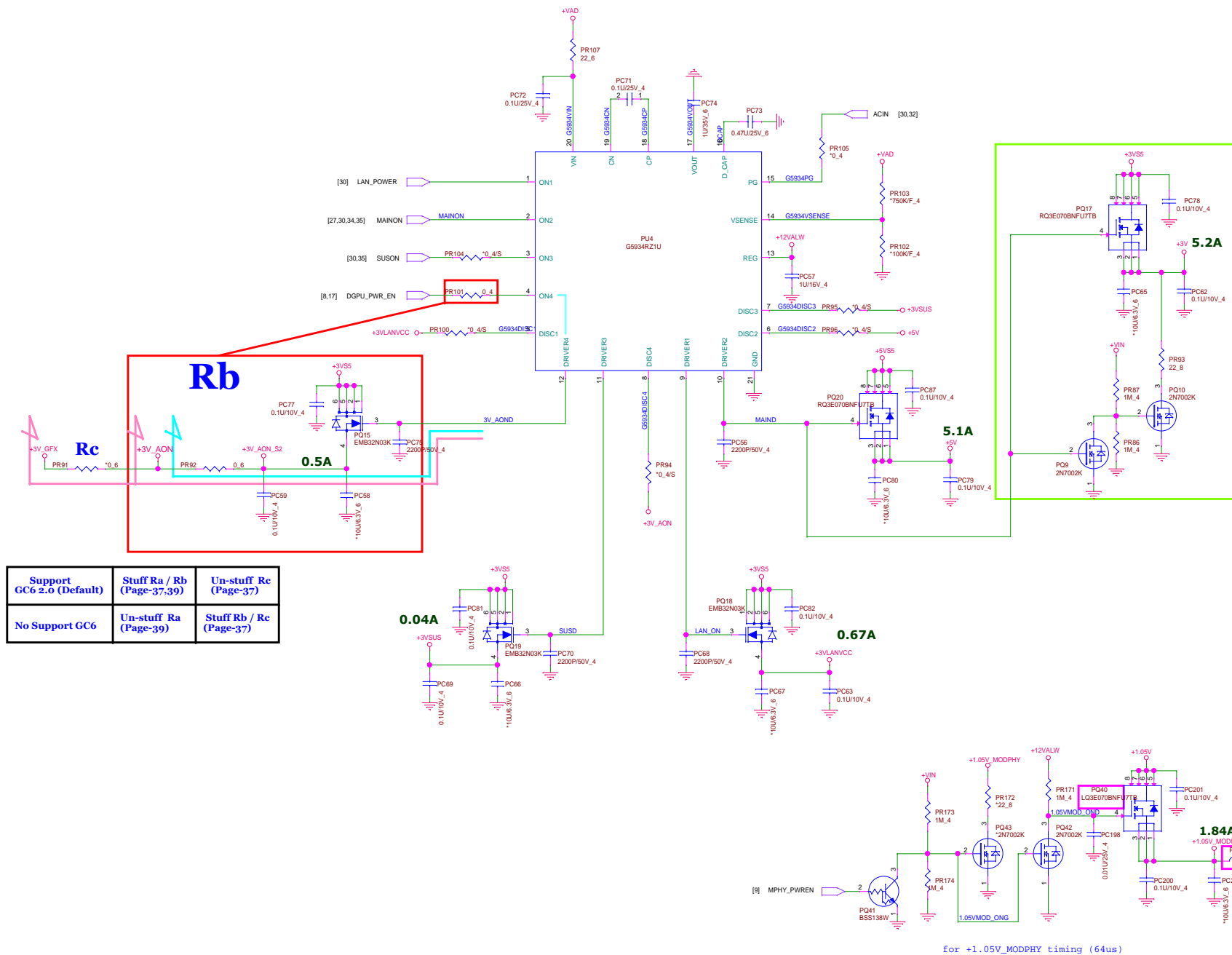
+VIN [20,31,32,33,35,36,37,38,39,40]
+3VS5 [6,9,10,11,22,25,28,31,33,37,39]
+5VS5 [13,22,27,31,33,35,36,37,38,40]
+5VPCU [13,33]

+VIN [20,31,32,33,34,36,37,38,39,40]
 +5VS5 [13,22,27,31,33,36,37,38,40]
 +1.35VSUS [2,4,12,13,31]



	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



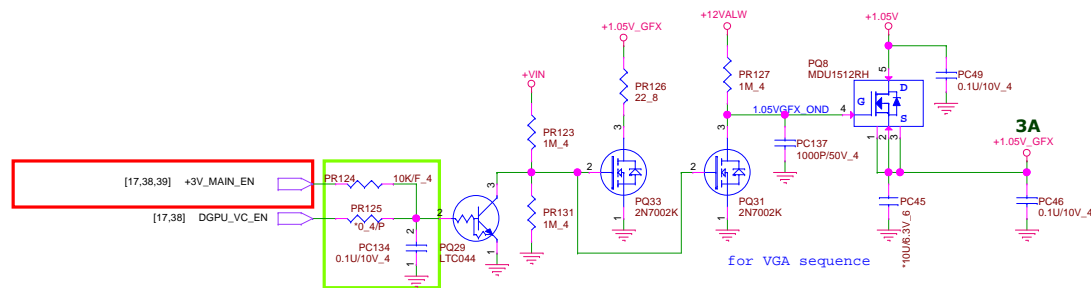
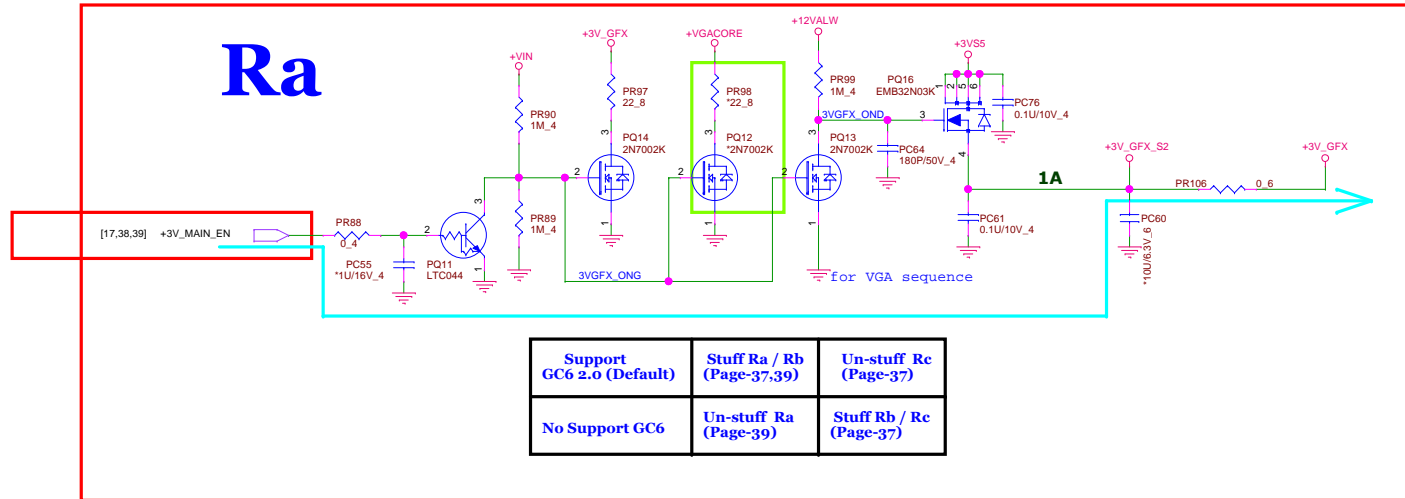


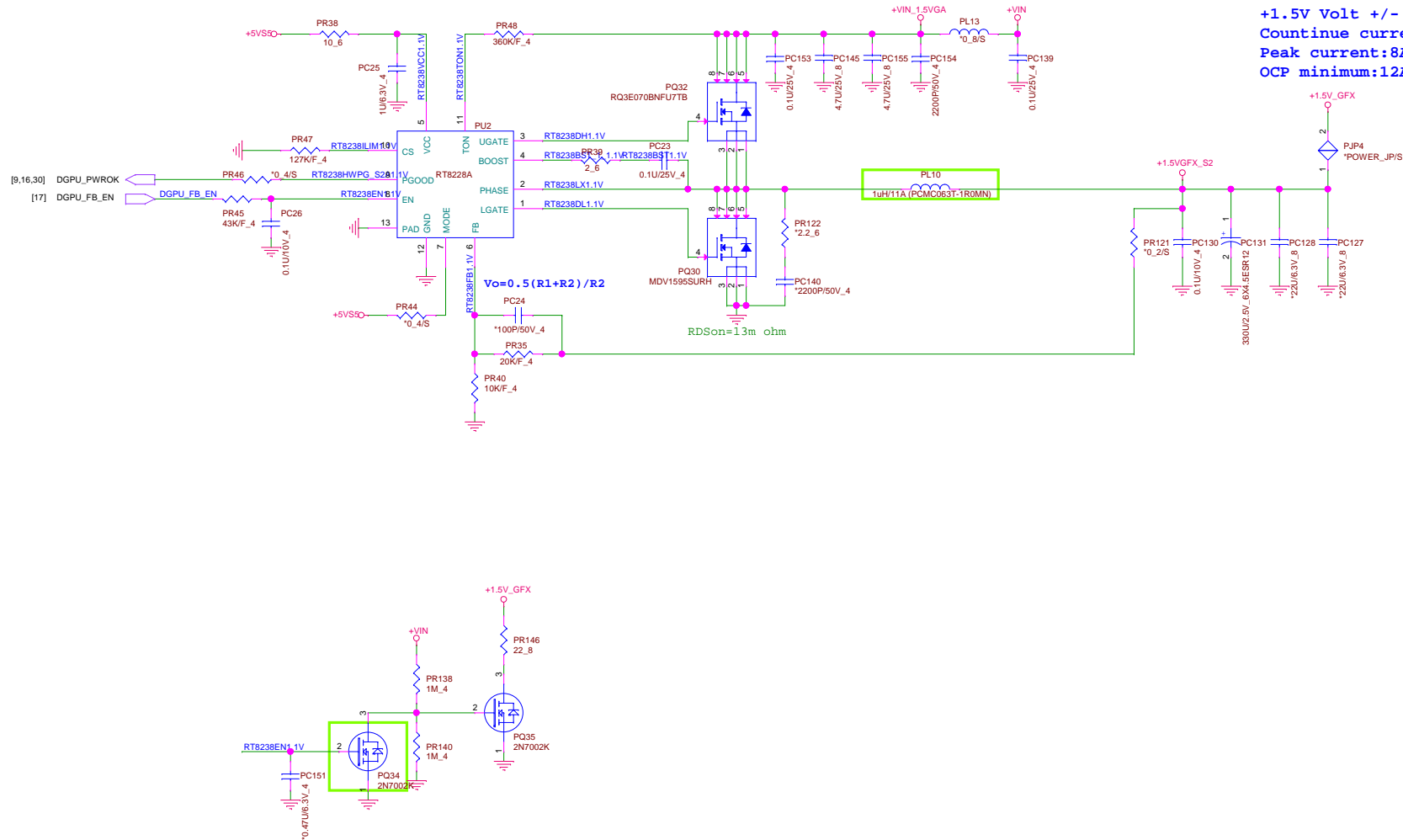
Support GC6 2.0 (Default)	Stuff Ra / Rb (Page-37,39)	Un-stuff Rc (Page-37)
No Support GC6	Un-stuff Ra (Page-39)	Stuff Rb / Rc (Page-37)

for +1.05V_MODPHY timing (64us)

38







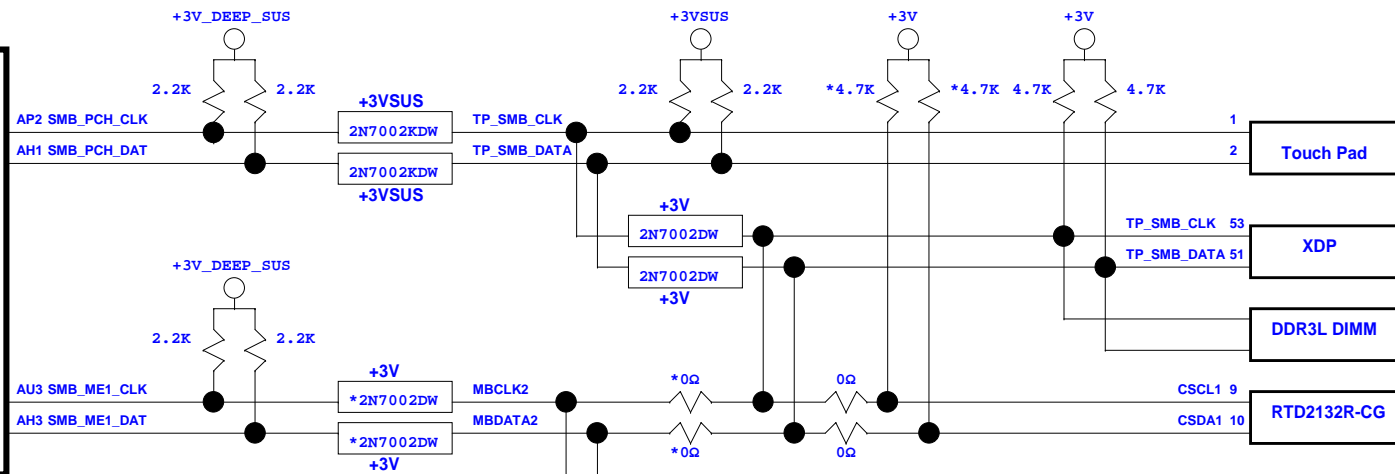
USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT3	NC	N/A
PORT4	NC	N/A

USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON#(from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON(from EC)

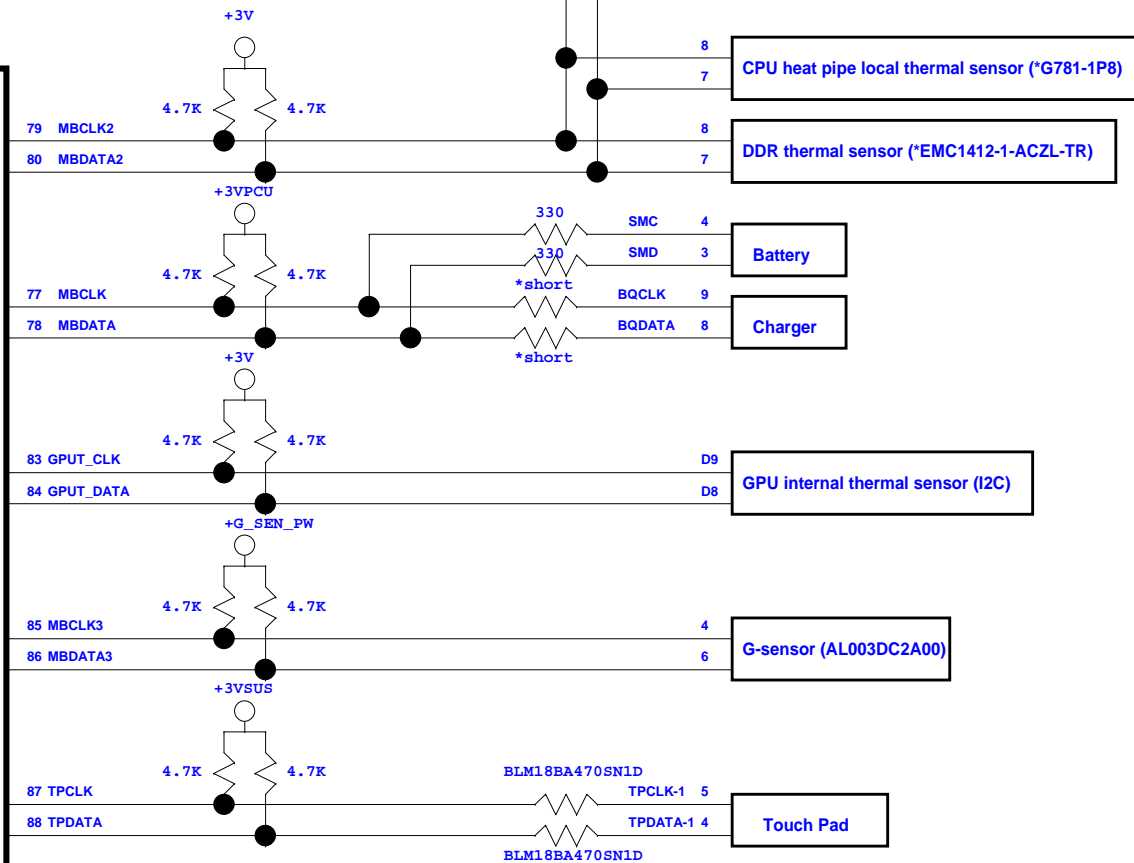
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	mSATA	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	

Haswell
ULT



EC
KB9010QF



TWB+JWV SYSTEM POWER BLOCK DIAGRAM

